Avoiding Dispersion in Distributed RLC Lines by Shaping

Jaijeet S. Roychowdhury

AT&T Bell Laboratories, Allentown, PA

Abstract

The shaping of RLC lines for delay reduction is investigated. It is shown that inductance can act to diminish dispersion, to the extent of reducing delay to its theoretical time-of-flight minimum even in the presence of substantial loss in the line. Simulations predict significant delay improvement (25%-38%) for long MCM lines propagating high-speed signals.

1 Introduction

It has been demonstrated that delay reduction is possible by shaping wires modelled as RC segments [CLZ93]. Recently, the stronger result that the exponential taper is optimal for minimizing Elmore delay in distributed RC lines has been proved [FS94]. In this paper, the effect of shaping on the delay of wires with distributed inductance, in addition to resistance and capacitance, is investigated.

The inclusion of inductance is motivated by the well-known fact that inductive effects become significant for long MCM interconnect propagating high-speed signals. Qualitatively, the distributed RLC case differs from the RC case in that the inductance makes peaking and oscillations possible, and models time-of-flight delays that can be significant at high speeds. The advantage of peaking is that it can lead to smaller rise/fall times; the disadvantage is that it may result in undesirable oscillations. It is shown in this work that it is possible to retain the advantages while diminishing or eliminating the disadvantages. Use is made of the loss (resistance) of the line. The desirable effects of loss (that it kills reflections and oscillations) are used to advantage, while the undesirable ones (that it slows rising/falling edges, an effect known as *dispersion*[1]) are alleviated by heightening the initial peaking response through tapering. Experimental simulations suggest that the technique can be useful for long MCM interconnections operating at high speeds.

The elegant result that the exponential taper is optimal for the RC case was demonstrated [FS94] by solving the Euler-Lagrange equations of the calculus of variations, minimizing the Elmore delay over all possible shapes of the distributed line. It is shown in Section 2 that the Elmore delay (first moment) is not altered by the inclusion of inductance. Thus the results of [FS94] carry over to the distributed RLC case. Unfortunately, the first moment is not a good measure of delay for the RLC case, unlike for the RC case in which it is known to provide a good empirical metric. A new measure, effective for resistively terminated RLC lines, is defined in Section 3. Using this measure, a quantitative understanding of the delay improvement possible by shaping is obtained for the case of resistive termination. The surprising fact that it is possible to *entirely eliminate* loss-induced delay leaving only the "lossless" or time-of-flight delay, is demonstrated for the resistive termination case. This case also suggests a bound on the delay improvement possible for the more useful case of capacitive termination, for which theoretical results are not available yet. In Section 4, simulations are presented that demonstrate delay improvements for capacitive terminations.

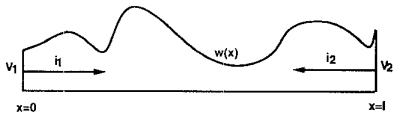

Figure 1: Tapered line

2 First Moment is Independent of Inductance

Consider the arbitrarily tapered line shown in Fig. 1. Let $w(x)$ represent the width of the line at point x along its length, and let l be its total length.

Let $R(x)$, $L(x)$ and $C(x)$ denote the resistance, inductance and capacitance at the point x. These are related to the width of the line at x. Assuming that the transverse dimensions of the line are small compared to the length, and neglecting fringing capacitance, the following expressions hold [GK68]:

$$R(x) = \frac{R_0}{w(x)}, \quad L(x) = \frac{L_0}{w(x)}, \quad C(x) = C_0 w(x) \tag{1}$$

Consider the circuit shown in Fig. 2, with Z_L set be be a capacitance, $\frac{1}{sC_L}$. Denoting by $V = V(x,s)$ the Laplace transform of the voltage at the point x, it can be shown [GK68] that the following differential equation holds:

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial V}{\partial x}\frac{\frac{\partial w}{\partial x}}{w} - sC(0)\left[sL(0) + R(0)\right]V = 0 \tag{2}$$

The boundary conditions imposed by the circuit are:

$$\frac{E - V(0)}{Z_S} = I(0) = -\frac{1}{sL(0) + R(0)}\left.\frac{\partial V}{\partial x}\right|_{x=0} \tag{3}$$

[1] Also called *diffusion delay* or just *distortion* (not to be confused with *harmonic distortion*).

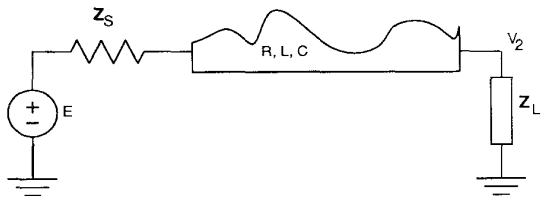

Figure 2: Circuit for delay calculation

$$V(l)sC_L = I(l) = \frac{1}{sL(0)+R(0)} \frac{w(l)}{w(0)} \left.\frac{\partial V}{\partial x}\right|_{x=l} \tag{4}$$

Consider the transfer function $H(x,s) = \frac{V(x,s)}{E(s)}$. Dividing Equation 2 by E(s):

$$\frac{\partial^2 H}{\partial x^2} + \frac{\partial H}{\partial x}\frac{\frac{\partial w}{\partial x}}{w} - sC(0)\left[sL(0)+R(0)\right]H = 0 \tag{5}$$

Since the quantity of interest is the first moment of the transfer function, $H'(x,s) = \frac{\partial H}{\partial s}$, Equation 5 is differentiated with respect to s:

$$\frac{\partial^2 H'}{\partial x^2} + \frac{\partial H'}{\partial x}\frac{\frac{\partial w}{\partial x}}{w} - H'sC(0)[sL(0)+R(0)] - HC(0)[R(0)+2sL(0)] = 0 \tag{6}$$

Evaluating at $s = 0$,

$$\left.\frac{\partial^2 H'}{\partial x^2}\right|_{s=0} + \left.\frac{\partial H'}{\partial x}\right|_{s=0}\frac{\frac{\partial w}{\partial x}}{w} - H|_{s=0}R(0)C(0) = 0 \tag{7}$$

$H(s)|_{s=0}$ is the transfer function at DC, which is unity because the load is capacitive; hence (denoting $H'|_{s=0}$ by H'_0):

$$\frac{\partial^2 H'_0}{\partial x^2} + \frac{\partial H'_0}{\partial x}\frac{\frac{\partial w}{\partial x}}{w} = R(0)C(0) \tag{8}$$

Similarly, by dividing the boundary conditions (Equations 3 and 4) by $E(s)$, differentiating w.r.t s, and evaluating at $s = 0$, the following boundary conditions for Equation 8 are obtained:

$$\frac{-R(0)}{Z_S}H'_0(0) = \left.\frac{\partial H'_0}{\partial x}\right|_{x=0} \tag{9}$$

$$H'_0(l)R(0)C_L = \frac{w(l)}{w(0)}\left.\frac{\partial H'_0}{\partial x}\right|_{x=l} \tag{10}$$

Note that the inductance L does not appear anywhere in Equation 8 or its boundary conditions Equations 9 and 10. Since these three equations together specify $H'_0(x)$ uniquely in the interval $0 \le x \le l$, it is clear that $H'_0(x)$ in general and $H'_0(l)$ in particular do not depend on the inductance in the line. This first moment is the same as in a line without inductance modelled, i.e., a distributed RC line, therefore the results in [FS94] apply equally to the optimization of the first moment of the distributed RLC line.

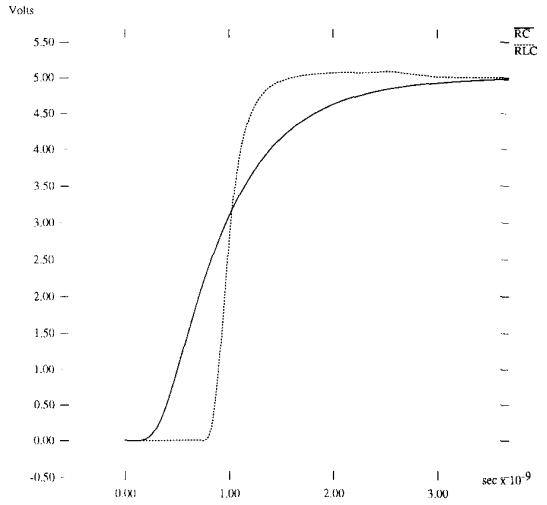

Figure 3: RC vs. RLC

The fact that the first moment of the transmitted waveform is not altered by the inductance of the line does not imply that the two waveforms are the same. Fig. 3 displays the difference that results from neglecting the inductance of a tapered distributed line with an 8:1 taper between the sending and receiving end. The RC model neglects the time-of-flight delay of the line, and overestimates the 90% rise point by about 50%. This indicates that the first moment or Elmore delay, which has proven to be a good estimate of delay for RC lines, is not so for RLC lines.

3 Avoiding Dispersion by Tapering

It is shown in this section that the inductance of a distributed line can reduce propagation delay to its theoretical minimum (the time-of-flight delay) even in the presence of distributed resistance and capacitance. This surprising result is derived by considering an exponentially tapered line terminated by a resistive load. A criterion that measures the transmission fidelity of fast edges is obtained by finding the impulsive component of the impulse response of the resistively terminated line. The use of this criterion is demonstrated using a simple example.

3.1 Impulsive Component of Impulse Response

Consider a distributed RLC line with an exponential shape, i.e.,

$$w(x) = w_0 e^{cx}, \qquad 0 \le x \le l \tag{11}$$

where c is the taper factor of the line and l its total length. Equations 1 imply that the products RC and LC are independent of x, therefore can be denoted by the following constants:

$$d = R(x)C(x), \quad k^2 = L(x)C(x) \tag{12}$$

It can be shown [GK68] that the Laplace-domain equations relating the terminal voltages $V_1(s)$, $V_2(s)$ and currents $I_1(s)$, $I_2(s)$ of the exponentially tapered transmission line are:

$$e^{\frac{c}{2}l}\left[V_2\left(\gamma-\frac{c}{2}\right)-\left(sL(l)+R(l)\right)I_2\right] = e^{-\gamma l}\left[V_1\left(\gamma-\frac{c}{2}\right)+\left(sL(0)+R(0)\right)I_1\right] \quad (13)$$

$$e^{-\frac{c}{2}l}\left[V_1\left(\gamma+\frac{c}{2}\right)-\left(sL(0)+R(0)\right)I_1\right] = e^{-\gamma l}\left[V_2\left(\gamma+\frac{c}{2}\right)+\left(sL(l)+R(0)\right)I_2\right] \quad (14)$$

where γ is defined as:

$$\gamma(s)=\sqrt{s^2k^2+sd+\frac{c^2}{4}} \quad (15)$$

To analyze transmission delay, Equations 13 and 14 are applied to the circuit in Fig. 2. The following expression is obtained for the output voltage in terms of the input:

$$\frac{V_2}{E}(s)=\frac{2\gamma e^{-\gamma l}e^{-\frac{c}{2}l}\left[sL(0)+R(0)\right]}{Z_S D(s)} \quad (16)$$

$$D(s)=\left[(\gamma-\tfrac{c}{2})+\tfrac{sL(l)+R(l)}{Z_L}\right]\left[(\gamma+\tfrac{c}{2})+\tfrac{sL(0)+R(0)}{Z_S}\right] - e^{-2\gamma l}\left[(\gamma+\tfrac{c}{2})-\tfrac{sL(l)+R(l)}{Z_L}\right]\left[(\gamma-\tfrac{c}{2})-\tfrac{sL(0)+R(0)}{Z_S}\right] \quad (17)$$

By dividing the numerator and denominator of Equation 16 by the first term of $D(s)$ (Equation 17), the following form is obtained for the transfer function:

$$\frac{V_2}{E}(s)=\frac{f(s)}{1-g(s)} \quad (18)$$

$$f(s)=\frac{2\gamma e^{-\gamma l}e^{-\frac{c}{2}l}\left[sL(0)+R(0)\right]}{Z_S\left[(\gamma-\frac{c}{2})+\frac{sL(l)+R(l)}{Z_L}\right]\left[(\gamma+\frac{c}{2})+\frac{sL(0)+R(0)}{Z_S}\right]} \quad (19)$$

$$g(s)=\frac{e^{-2\gamma l}\left[(\gamma+\frac{c}{2})-\frac{sL(l)+R(l)}{Z_L}\right]\left[(\gamma-\frac{c}{2})-\frac{sL(0)+R(0)}{Z_S}\right]}{\left[(\gamma-\frac{c}{2})+\frac{sL(l)+R(l)}{Z_L}\right]\left[(\gamma+\frac{c}{2})+\frac{sL(0)+R(0)}{Z_S}\right]} \quad (20)$$

The denominator of Equation 18 can be expanded in a binomial expansion to obtain:

$$\frac{V_2}{E}(s)=f(s)\left[1+g(s)+g^2(s)+g^3(s)+\cdots\right] \quad (21)$$

Note that $f(s)$ has an $e^{-\gamma l}$ term, and $g(s)$ contains an $e^{-2\gamma l}$ term. It can be shown that the Laplace-inverse $e^{-\gamma l}$ has a delay of $T=kl$ in the time domain (i.e., the inverse transform of $e^{-\gamma l}$ is identically zero for $t<T$). T is the time-of-flight delay of the line. Each term $g^i(s)$ in Equation 21 corresponds to a reflection that appears only after $t=(2i+1)T$ (a delay of $2iT$ from $g^i(s)$, and T from $f(s)$). The first term has only an $f(s)$ contribution, accounting for the transmission of the signal with a time-of-flight delay of T. The term of primary interest is therefore the first, $f(s)$; in addition, it is desirable to reduce the reflective effects represented by the $g(s)$ terms.

In general, the inverse transform of the first term $f(s)$ consists of an impulsive component at $t=T$, plus a non-impulsive response that is nonzero for $t\geq T$. The impulsive component leads to a faithful reproduction of the input signal at the output, delayed but without dispersion; whereas the non-impulsive part slows rise/fall times by distorting the waveform. In order to improve delay, the impulsive component of $f(s)$ needs to be estimated and manipulated by tapering.

If Z_S and Z_L are resistive as assumed, this component, denoted by M, is obtained by shifting $f(s)$ to the left by T (in the time domain) and using the initial value theorem for Laplace transforms (derivation not shown):

$$M=\frac{2e^{-\frac{c}{2}l}e^{\frac{-cl}{2k}}kL_0}{Z_S w_0\left[k+\frac{L_0e^{-cl}}{Z_L w_0}\right]\left[k+\frac{L_0}{Z_S w_0}\right]} \quad (22)$$

3.2 Example of Delay Improvement by Tapering

The significance of the quantity M derived above is that sharp edges of the input signal are transmitted with gain M, without deterioration in rise/fall time but with a delay equal to the time-of-flight T. It is desirable to have $M=1$. Long lossy lines that are *uniform* (i.e., $c=0$) suffer from having $M<1$, with the result that the output waveform rises quickly to only a fraction of the input level, followed by a slower rise qualitatively similar to that of RC charging. Useful insight is obtained by considering the simplified situation of $Z_L=\infty$, the case of a lossy line terminated by an open circuit. In this case, M simplifies to:

$$M=\frac{2L_0}{L_0+Z_S k w_0}e^{-\frac{c}{2}l}e^{\frac{-dl}{2k}}\delta(t-T) \quad (23)$$

If Z_S is chosen to be $\frac{L_0}{kw_0}=\sqrt{\frac{L(0)}{C(0)}}$, the characteristic impedance of the $x=0$ end of the line, the first term in Equation 23 becomes 1, and only the two exponential terms are left. The first exponential term is a factor due to the taper c, whereas the second is an attenuation due to the loss factor d. In a uniform line $c=0$, leaving only the loss term which is always less than 1, leading to a diminishing of the fast-changing part of the transmitted signal[2]. By setting $c<0$ (i.e., tapering to make the line thinner as x increases), however, the *attenuation due to the loss can be compensated by the taper factor* $e^{-\frac{c}{2}l}$, bringing the value of M back to the desired 1. Note also that uniform sizing, which translates to manipulating w_0 in Equation 23, can contribute at best a factor of 2 via the first term, whereas the taper factor is not similarly limited.

This is illustrated by the simulation shown in Fig. 4. The parameters of the interconnect (for the uniform case) were obtained from [NCFH88][3]; Z_S was set to 70Ω. The

[2] A best-case factor of 2 can be gained from the first term in Equation 23 by having $Z_S=0$; but as seen in the examples in Section 4. even this may not be sufficient to bring M up to 1.

[3] $C=0.468$pF, $R=12.45\Omega$, $L=8.792$nH, per cm; 16 cms long.

input signal (not shown) has a rise-time of 200ps and an amplitude of 5V. The uniform line has M equal to approximately 0.65, which is the level to which the waveform rises quickly; after which dispersion sets in and the waveform rises slowly. The line with the 4:1 taper ($c = -0.087$) has $M \approx 1$, leading to a near-perfect waveform. The more aggressive 8:1 taper ($c = -0.13$) has $M \approx 1.2$ leading to an overshoot, followed by dispersion in the opposite direction. The time-of-flight delay $T \approx 1ns$ is evident in all cases; also, the effects of the first reflection (at about 3ns), as evidenced by the small kinks, can be seen to have been reduced to negligible amounts by the loss of the line.

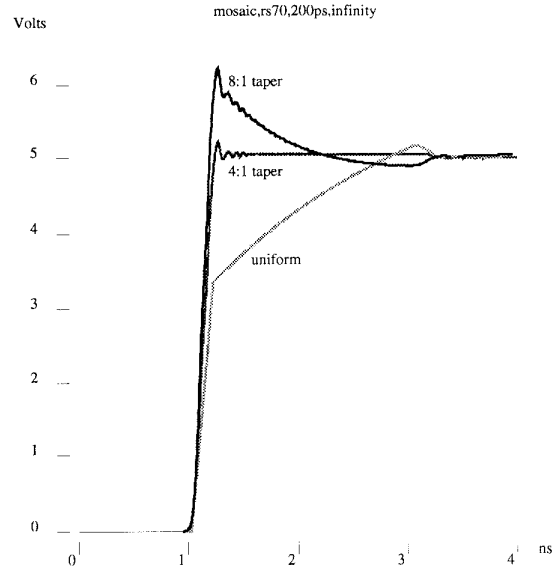

Figure 4: Simulation of the effects of taper with $Z_L = \infty$

For nonzero loads ($Z_L < \infty$), it can be shown that an optimal taper exists that maximizes M. If $M >= 1$ at the optimal taper, loss-induced delay can be eliminated entirely by shaping.

The above example suggests that making the line thinner in the direction of signal transfer may improve the quality of the transmitted pulse even for the more general case of capacitive loading. This is considerably more difficult to analyze than the resistive case. Estimating the impulse strength M cannot be used, as M (Equation 22) can be shown to be always zero when Z_L is capacitive, i.e., there is no impulsive component in the transfer function. Instead, the impulsive component is "spread out" into a non-impulsive response that becomes sharper as $Z_L = \frac{1}{sC_L}$ is increased, approaching an impulse as $C_L \rightarrow 0$. With a finite value of C_L, the rising/falling edges of the transmitted signal resemble, qualitatively, a waveform with two time constants: the faster being a replacement of the impulsive component of the resistive loading case, and the slower due to dispersion (see the figures in Section 4). Using the poles of $\frac{V_2}{E}$ for analyzing the capacitive loading case is currently under investigation.

4 Experimental Results

In this section, examples are presented that demonstrate that tapering RLC lines can be useful for capacitive loading. Interconnect is considered from a square MCM of 5cm side. Instead of the usual 10% to 90% delay, a more conservative 0% to 90% delay measure is used for convenience to derive numerical values for delay. Note that all delay numbers *include time-of-flight delays*.

Two cases, with line lengths of 5cm and 10cm, are considered. For each case, two values of Z_S are used: low (lower bound for driver output resistance) and high (upper bound). The load capacitance is fixed at 1pF unless otherwise noted, and the input waveform, which starts at $t = 0$, is a step with a rise time of 200ps and an amplitude of 5V.

For each value of Z_S, three tapers are used: uniform, 4:1 and 8:1.

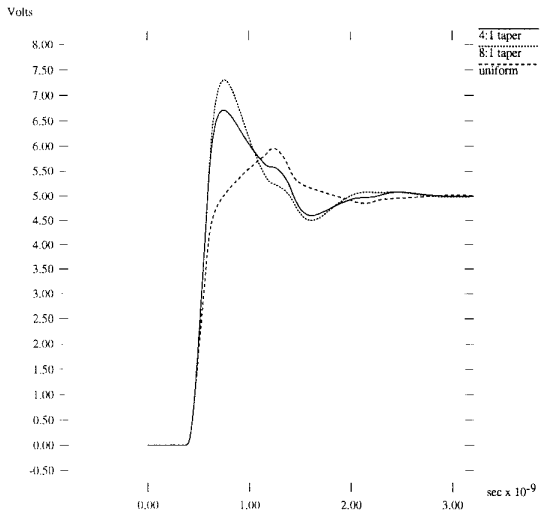

Figure 5: 5cm, low Z_S, Z_L=1pF

In Fig. 5, output waveforms for the 5cm line with low Z_S are shown. As can be seen, the uniform taper has an overshoot, which is heightened by tapering to 4:1 and 8:1. For this case, the tapering provides no appreciable improvement in delay as all three waveforms are almost identical up to the 4.5V (90%) mark. The ringing observed in all three waveforms, especially at sharper tapers, is not of major concern as gates usually have diode clamps that eliminate its adverse effects. Fig. 6 illustrates the effect of a diode clamp to 5V at the load. The heightening of the overshoot caused by tapering can be observed.

In Fig. 7, the outputs of the 5cm line for high Z_S are shown. It can be seen that the uniform case becomes dispersion limited at about 3.5V. The 4:1 taper leads to a waveform that is much sharper at higher values, while the 8:1 taper maintains the sharpness and displays a small overshoot. Both tapers reduce the delay to the time-of-flight value, an overall improvement of about 33%. Note that the percentage reduction in *loss-induced delay* alone is much

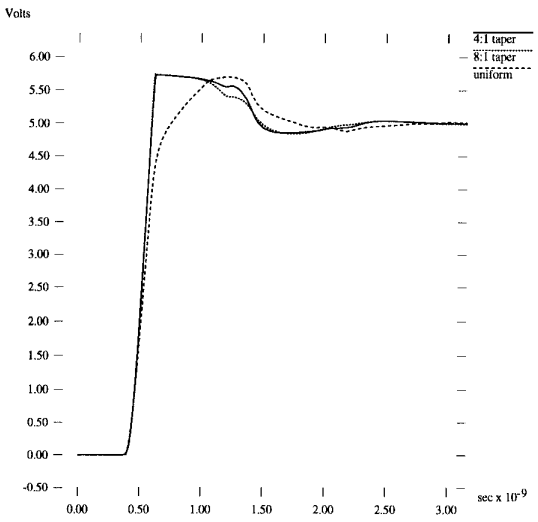

Figure 6: 5cm, low Z_S, Z_L=1pF, diode clamp

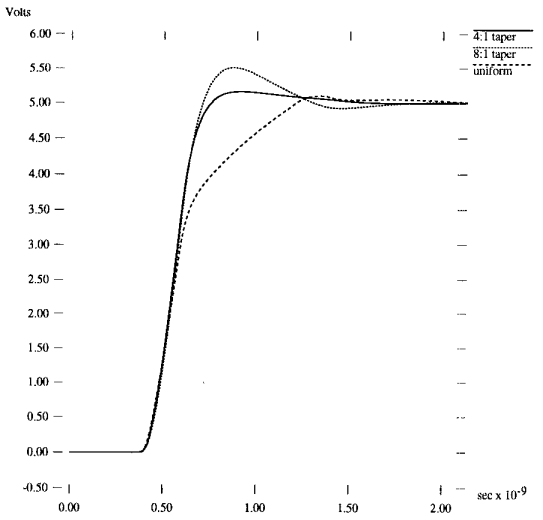

Figure 7: 5cm, high Z_S, Z_L=1pF

greater as it is essentially eliminated, the remaining delay being the time taken for light to carry the signal through the length of the line. With an increase in the load capacitance to 2pF, the results remain qualitatively similar (Fig. 8); the delay reduction in this case is about 25%. This demonstrates that the worst-case delay over Z_S variations is improved by 25%-33% using the 8:1 taper.

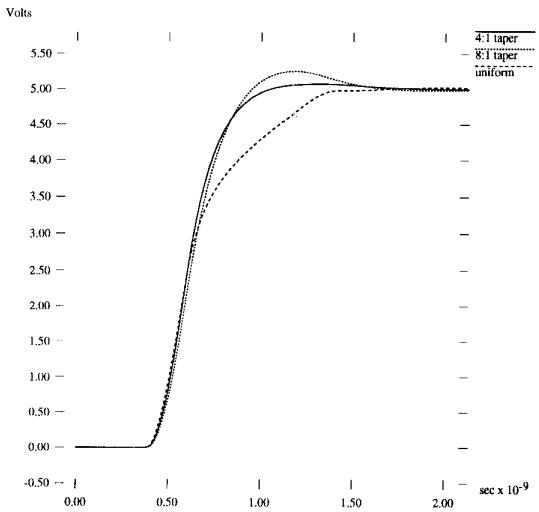

Figure 8: 5cm, high Z_S, Z_L=2pF

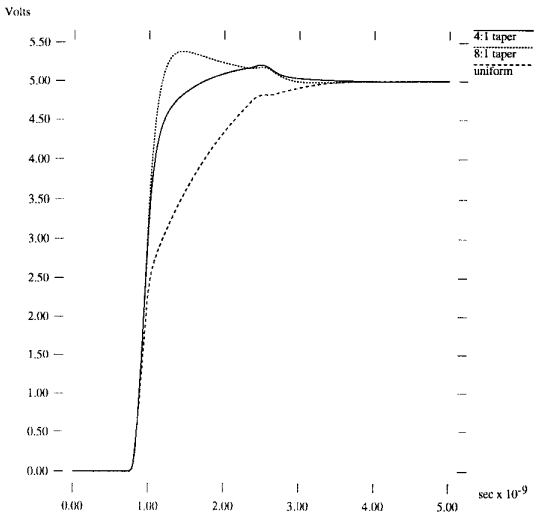

Figure 9: 10cm, low Z_S, Z_L=1pF

The next two figures illustrate the result of tapering the longer line of 10cm. The low Z_S case is shown in Fig. 9. The 4:1 taper leads to a delay reduction of about 43% while the 8:1 taper leads to approximately 47% - both reduce the

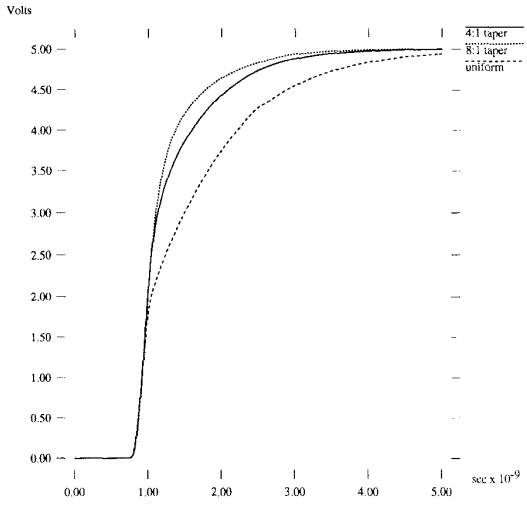

Figure 10: 10cm, high Z_S, Z_L=1pF

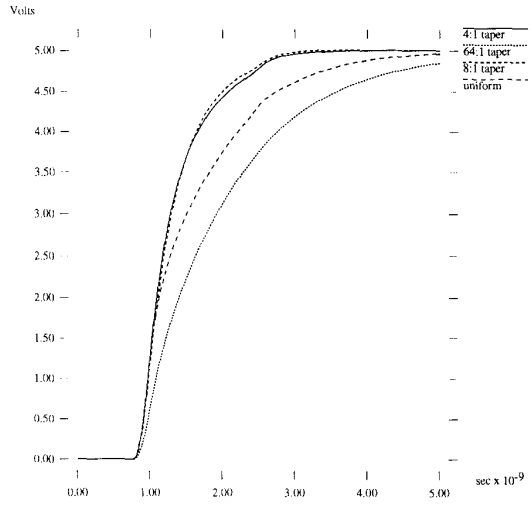

Figure 11: 10cm, low Z_S, Z_L=4pF

delay to close to its time-of-flight minimum. For the high Z_S case (Fig. 10), the improvements are 27% and 38% respectively for the 4:1 and 8:1 tapers. The improvement in worst-case delay over Z_S variation is thus about 38%.

It may appear from the above that making the taper sharper always improves delay, limited only by fringing capacitance and manufacturability. This is however not true, as illustrated in Fig. 11, in which the line length is 10cm, Z_S is low, and the load capacitance has been increased to 4pF. While the 4:1 and 8:1 tapers produce nearly identical results with a delay reduction of about 27%, using a 64:1 taper results in a large increase in delay instead of a reduction. This suggests that an optimal taper exists when the load is capacitive; it is known that this is so for the distributed RC line [FS94] and for the distributed RLC line with resistive termination (as shown in the previous section).

5 Conclusion

It has been shown that tapering distributed RLC lines can lead to improved delay through the peaking effect caused by inductance. Simulations of realistic MCM interconnect situations confirm delay reduction through tapering.

Current work is focussed on developing an analytical technique for predicting the optimal taper when the line is capacitively loaded.

Acknowledgments

The author would like to thank R.C. Frye for providing interconnect parameters and R.C. Melville for acting as reviewer. Support from S. Liu, K. Singhal and W.J. Evans is gratefully acknowledged.

References

[CLZ93] J. Cong, K.S. Leung, and D. Zhou. Performance-driven interconnect design based on distributed RC delay model. In *Proc. IEEE DAC*, pages 606–611, 1993.

[FS94] J.P. Fishburn and C.A. Schevon. Shaping a Distributed-RC line to Minimize Elmore Delay. Technical Report ITD-94-22770A, AT&T Bell Laboratories, 1994.

[GK68] M.S. Ghausi and J.J. Kelly. *Introduction to distributed-parameter networks; with application to integrated circuits*. Holt, Rinehart and Winston, New York, 1968.

[NCFH88] C.A. Neugebauer, R.O. Carlson, R.A. Fillion, and T.R. Haller. High Performance Interconnections between VLSI Chips. *Solid State Tech.*, June 1988.