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# Fast, accurate prediction of PLL jitter induced by power grid noise

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***Abstract*— Timing jitter caused by power supply fluctuations is an important concern in phase-locked loop (PLL) design. We present a novel technique for predicting supply-induced PLL timing jitter that is much more accurate than prior methods. Our method, based on a nonlinear VCO macromodel, is able to predict phase errors correctly where prior linear macromodels fail. The macromodel is easily extracted from SPICE-level descriptions of any oscillator or VCO. We demonstrate the proposed technique on a ring oscillator based PLL, providing comparisons against prior linear macromodels and against full SPICE-level simulations. Speedups of three orders of magnitude are obtained over full SPICE-level simulation, with larger speedups expected for PLLs with more devices and nodes.**

## I. INTRODUCTION

PLLs [1] are critical components in virtually all mixed-signal and digital systems. Their uses include clock and data recovery (CDR), frequency synthesis, direct-FM modulation, suppression of on-chip clock skew, *etc.*. A major performance problem for on-chip PLLs is timing jitter, caused by power supply and substrate noise from large blocks of switching digital circuits on the same chip. Noise in power supply and ground lines, caused by $IR$ and $L\frac{dI}{dt}$ drops [2]–[4], disturbs the PLL's voltage-controlled oscillator (VCO), resulting in phase errors. Supply-induced jitter has, in fact, become a dominant performance-limiting factor in deep submicron (DSM) designs [8]; hence, accurate and quick jitter prediction during design is extremely important for ensuring correct overall system functionality upon tape-out.

As is familiar to designers of PLLs, their simulation at the SPICE level can be extremely challenging and computationally intensive. This is especially so for jitter prediction, since it is necessary to first bring the PLL into lock and to then run small-noise simulations for long enough to obtain reasonable RMS jitter figures. Issues of controlling numerical noise and the inherent difficulty of simulating the embedded VCO (requiring very small time-steps) add to the problems of PLL simulation. Hence, there has been considerable interest in faster and more convenient methods for jitter simulation that do not, however, appreciably sacrifice accuracy.

A number of such approaches (*eg.*, [8]–[11]) have been proposed, often drawing on related techniques (*eg.*, [5]–[7]) for predicting phase noise in oscillators. These approaches are all based on using *simplified phase-domain macromodels* of the VCO, as well as of the other components of the PLL. In other words, SPICE-level descriptions of the PLL's components are replaced by simplified block system-level representations, typically developed manually with the aid of simulations of individual blocks. Furthermore, prior approaches all use *linear* macromodels to represent the impact of power-supply noise on the VCO (the primary contributor to PLL jitter). Most approaches further employ a simple linear time-invariant integral model to represent the effect of supply noise on jitter, although there do not appear to be any systematic studies available of errors introduced by linear approximations to the VCO's phase response.

In this paper, we first demonstrate that linear phase macromodels cannot predict phase error in VCOs/PLLs reliably, often resulting in large errors. We then propose a computationally efficient *nonlinear* jitter macromodel to replace linear ones and eliminate their shortcomings. The nonlinear jitter macromodel is based on the VCO's Perturbation Projection Vector (PPV), a concept originally developed in the context of a rigorous nonlinear theory for phase noise in oscillators [6], [12]. The PPV-based nonlinear jitter macromodel can be accurately and efficiently extracted from SPICE-level descriptions of the VCO [12]. We apply our nonlinear jitter macromodel to predict jitter in a ring oscillator based PLL, comparing results against full (SPICE-level) simulations, as well as against linear VCO jitter macromodels. We demonstrate that the nonlinear jitter macromodel predicts PLL timing jitter far more accurately than linear macromodels, while at the same time remaining much faster than full simulation (with speedups of 1000×).

We emphasize that the concepts behind our jitter calculation method are not identical to that of [7] and related approaches, which use the concept of a time-varying impulse sensitivity function (ISF). There are two key differences between [7] and our approach. Firstly, our method uses an accurate nonlinear phase equation to predict the jitter, in contrast to the linear (though time-varying) one of [7]. Secondly, the PPV function used in our method (which also captures the sensitivity of the VCO's phase to perturbations) is, in general, different from the ISF of [7] – especially for ring oscillators. As has been established [6], [13], using the ISF can lead to significant errors in phase error prediction, depending on the type of VCO used; the correct procedure is to use the PPV within a nonlinear phase error equation, as used in this work. In the following sections, we also provide comparisons with the linear ISF-based method and show that significant errors can result if even ISF-based linear techniques are applied to ring oscillators.

The remainder of the paper is organized as follows. In Section II, we review linear time-invariant VCO jitter macromodels and demonstrate that they do not capture PLL phase errors accurately. In Section III, we describe the nonlinear VCO phase macromodel and its use in PLL jitter prediction. Simulation results and comparisons for a ring-oscillator-based PLL are provided in Section IV.

## II. SHORTCOMINGS OF LINEAR VCO PHASE MACROMODELS

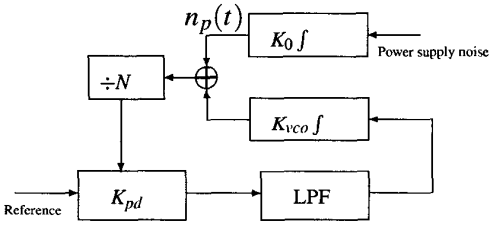


Fig. 1. Functional block diagram of a PLL.

Fig. 1 shows the diagram of a linear time invariant PLL macromodel. $K_{VCO}$ is the frequency sensitivity of the VCO to the control voltage from the low-pass filter, widely used in PLL phase analysis. $K_0$ is the frequency sensitivity of the VCO to the power supply [8]; it is typically estimated by applying different DC voltage perturbations to the power supply line, simulating the frequency of the VCO's oscillation, and estimating the slope of the voltage-frequency plot [8]. The phase error due to power supply noise can then be calculated by solving

$$\Delta\Phi = K_0 \int \Delta V_{ps}(t), \tag{1}$$

where $V_{ps}$ is the power supply noise voltage.

This linear phase macromodel assumes that frequency sensitivity to supply voltage is a constant, independent of time; however, this is not true for real oscillators. The solid line in Fig. 2(b) is the frequency sensitivity waveform of a 3-stage ring oscillator. The waveform is calculated by the PPV method to be introduced later in Section III. From inspection of the ring oscillator's output waveforms in Fig. 2(a) and the frequency sensitivity waveform in Fig. 2(b), it is obvious that the ring oscillator is very sensitive to power supply noise near its switching instants. $K_0$ of the linear phase model is the average of the sensitivity waveform shown in Fig. 2(b). In this oscillator, $K_0$ from averaging the frequency sensitivity is $7.75 \times 10^6$. However, the maximum frequency sensitivity is around $4.7 \times 10^8$, which is 60 times greater than $K_0$. Because of this large discrepancy, the linear time-invariant phase macromodel is unable to capture timing jitter due to the power supply noise accurately under all kinds of noise excitations.

The impulse sensitivity function (ISF) based method of [5] is an improvement over the traditional LTI linear phase macromodel. In



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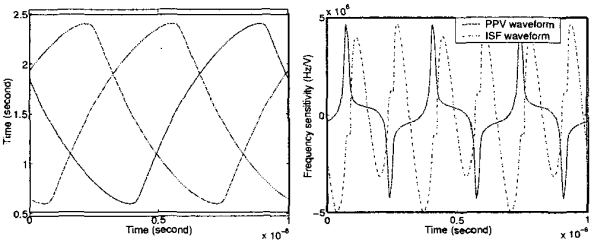
this method, the phase error due to noise is given by

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{\infty} \Gamma(\omega_0 \tau) i(\tau) d\tau, \quad (2)$$

where $q_{max}^k$ is the maximum charge displacement across the capacitor, $i(\tau)$ is the noise signal, and $\Gamma(\omega_0 \tau)$ is the impulse sensitivity function. The ISF is a periodic waveform which corresponds to the phase shift due to an impulse injected at time $t = \tau$. However, the ISF method suffers from two major drawbacks. Firstly, the ISF waveform calculated by the method described in [5] does not match the correct frequency sensitivity waveform well, as shown in Fig. 2(b). Secondly, the ISF method does not correctly account for the nonlinear generation of phase error. Nonlinearities arise essentially due to the frequency sensitivity waveform's being compressed or stretched due to phase fluctuations; the ISF method is unable to accurately predict such nonlinear phase shifts when phase fluctuations is rapid.




(a) (b)

Fig. 2. (a) The output waveform of a ring oscillator. (b) The frequency sensitivity to supply voltage of the oscillator

## III. A NONLINEAR VCO PHASE MACROMODEL FOR CAPTURING SUPPLY-GRID EFFECTS ON JITTER

To correctly account for the nonlinear dynamical nature of timing jitter generation in VCOs and PLLs, we adapt the nonlinear phase macromodel of [6] to develop a fast, accurate PLL jitter simulation capability.

The phase deviation $\alpha(t)$ due to the perturbation can be calculated by solving

$$\dot{\alpha}(t) = \mathrm{PPV}^T(t + \alpha(t)) \cdot b(t), \quad (3)$$

where $\mathrm{PPV}(t)$ is the perturbation projection vector (PPV), which captures the oscillator's phase sensitivity to perturbations. The PPV is a periodic vector waveform, with the same period as the unperturbed oscillator. $\alpha(t)$ in the nonlinear phase macromodel is the jitter, in units of time. The phase deviation (in radians) can be obtained by multiplying $\alpha(t)$ by the free-running oscillation frequency $\omega_0$. By solving (3) numerically, the phase error due to any perturbation can be computed. Note that since (3) is a scalar equation, its numerical solution is very rapid.

### A. Calculation of the PPV

The PPV can be extracted from a SPICE-level description of any oscillator using either time-domain or frequency-domain methods [6], [12]. We summarize the time-domain monodromy-matrix method for calculating the PPV.

1) Use any time-domain simulation tool to simulate the oscillator or VCO to obtain one cycle of its steady state $x_s(t)$. To minimize numerical errors, very small timesteps are usually necessary.
2) Linearize the oscillator equations over the steady-state waveform $x_s(t)$ as
$$C\dot{Y} = G(t)Y. \quad (4)$$
3) Compute the monodromy matrix $\Phi(T,0)$ by integrating (4) as a matrix differential equation, with initial value $Y(0) = I_n$.
4) Calculate $\dot{x}_s(t) = IFFT(j\Omega * FFT(x_s(t)))$ and use it as $u_1(t)$.
5) $v_1(0)$ is the eigenvector of $\Phi(T,0)^T$ corresponding to the eigenvalue 1.
6) Compute $v_1(t)$ for $0 < t < T$ by backward integration of the adjoint equation $C^T\dot{y} = -G^T(t)y$.
7) Calculate the scale factor using $S = \frac{1}{N}\sum v_1(i)^T u_1(i)$.
8) $\mathrm{PPV}(t) = \frac{1}{S} C^{-1} v_1(t)$.

### B. Using the nonlinear macromodel to predict phase error

Replacing the linear phase macromodel (1) with the nonlinear phase macromodel (3), we can accurately predict jitter given an appropriate supply noise waveform. In this paper, we analyze timing jitter in a PLL using both switching noise waveforms and sinusoidal noise waveforms.

Switching noise is generated by simultaneous switching of many gates in other circuit blocks that share (or otherwise affect) the power supply of the PLL. A simple elemental waveform, representative of switching noise, is a narrow triangular or trapezoidal waveform; in this paper, we employ a trapezoidal waveform.

Sinusoidal (or more generally, periodic) noise can result from other oscillators, clock generators or clock buffers that share the same power supply line. In addition, periodic gate switching of adjacent circuit blocks can also create sinusoidal/periodic noise. Such noise can be described as a sinusoidal waveform with an appropriate amplitude.

Since jitter in the VCO directly affects the PLL's output, we can easily derive the relationship between the intrinsic VCO jitter $n_{vco}(t)$ and the PLL's jitter $\phi(t)$ from Fig. 1, *ie.*,

$$\Phi(s) = \frac{1}{1 - \frac{1}{N} K_{pd} \frac{K_{vco}}{s} H_{LPF}(s)} N_{vco}(s), \quad (5)$$

where $H_{LPF}(s)$ is the transfer function of the low-pass filter. (5) can be expressed as the linear differential equation

$$\sum_{i=0}^{n} a_i \phi^{(i)}(t) = \sum_{i=1}^{n} b_i n_{vco}^{(i)}(t). \quad (6)$$

Combining (6) with the nonlinear phase macromodel (3), PLL jitter due to power supply noise is governed by the nonlinear differential equations

$$\begin{aligned} \dot{\alpha}(t) &= \mathrm{ppv}_{\mathrm{power}}(t + \phi(t)) \cdot b_p(t) \\ \textstyle\sum_{i=0}^{n} a_i \phi^{(i)}(t) &= \textstyle\sum_{i=1}^{n} b_i \alpha^{(i)}(t) \end{aligned} \quad (7)$$

where $ppv_{power}(t)$ is the PPV of the power supply node, and $b_p(t)$ is the power supply noise. (7) is a two-dimension nonlinear differential equation, which can be efficiently solved by numerical method.

## IV. APPLYING THE NONLINEAR VCO MACROMODEL TO PREDICT PLL JITTER

In this section, we use the nonlinear phase macromodel of Section III to predict jitter in a PLL employing the three-stage ring oscillator shown in Fig. 3. The PLL has a center frequency $f_0 = 100MHz$ and employs a low-pass filter with a dual RC pole at $R_f C_f = \frac{10^8}{5\pi} Hz$. The power supply line was modelled with a series resistance $R_p = 50$ and a decoupling capacitance of $C_p = 2pF$.

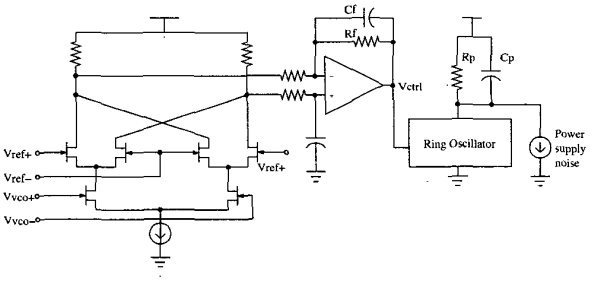



Fig. 3. Diagram of ring-oscillator based PLL.



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### A. Calculation of the PPV

The method of Section III is used to calculate the PPV of the ring oscillator VCO. The PPV is a group of periodic waveforms; each waveform represents the PLL's frequency sensitivity to any current injected from each circuit node. Fig. 4 shows the PPV components of the power supply node and the control node of the VCO. It is apparent from these waveforms that jitter in the VCO is most sensitive to power supply noise when the inverters are about to switch, and that it is most sensitive to noise in the control node right after the inverters have switched.

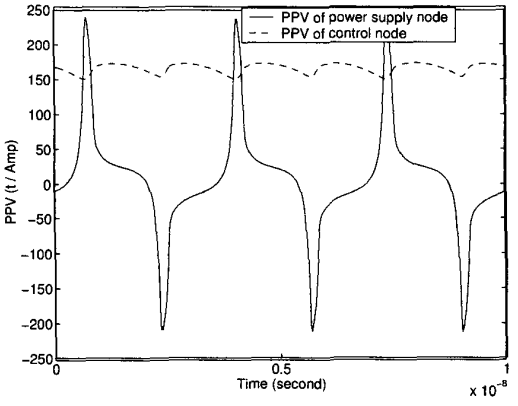


Fig. 4. The PPV of power supply node and control node

### B. Prediction of the impact of switching noise on jitter

As mentioned earlier, switching noise can be modelled as a train of trapezoidal waveforms with different amplitudes and start times. When the amplitude of switching noise is not large, the jitter induced can be considered to be roughly proportional to this amplitude. In this paper, we focus on the relationship between the jitter and the start time of the switching noise. We apply a single trapezoidal waveform, with maximum amplitude $A = 0.3mA$, to the PLL at different start times, and measure the jitter induced. The width of the switching noise waveform is 10% of the VCO's period.

To insure that our PLL macromodel is correct, we first inject switching noise to the PLL, and calculate the phase shift using both the nonlinear phase macromodel as well as full simulation. Fig. 5 shows the PLL's response to switching noise. It can be seen that the nonlinear jitter macromodel matches full simulation well, implying that the VCO phase macromodel, as well as the PLL system-level model itself, are both accurate.

We then repeatedly apply the single trapezoidal waveform to the PLL at different start time, measuring the maximum phase shift or jitter. Fig. 6 shows the relationship between the maximum timming jitter and the start time of the injected trapezoidal waveform. In Fig. 6, the timing jitter changes dramatically as time progresses, indicating that the jitter due to switching noise is highly dependent on when the noise is applied to the PLL. Again, our nonlinear macromodel matches the full simulation well. Results from using traditional linear time-invariant models, in contrast, do not compare well with full simulation at all. The ISF-based linear model, as presented in [5], also produces very small jitter numbers under the same switching noise. To make the most generous comparisons possible, we scale the ISF to match one point of the jitter waveform produced by full simulation; even so, as can be seen, the ISF-generated waveform does not match the full simulation well over the period.

### C. Prediction of the impact of periodic noise on jitter

Periodic noise cannot be completely eliminated by the feedback mechanism inherent to the PLL, because of the low pass filter's bandwidth limitation. Jitter in the VCO caused by periodic (*eg.*, sinusoidal) noise depends strongly on the frequency of the sinusoid. This is easily explained by the nonlinear phase model. In (3), the phase shift $\alpha(t)$ grows with a slope which equals the product of

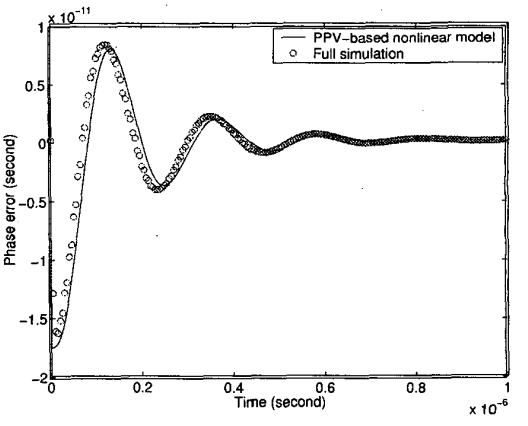


Fig. 5. The impulse response of the PLL

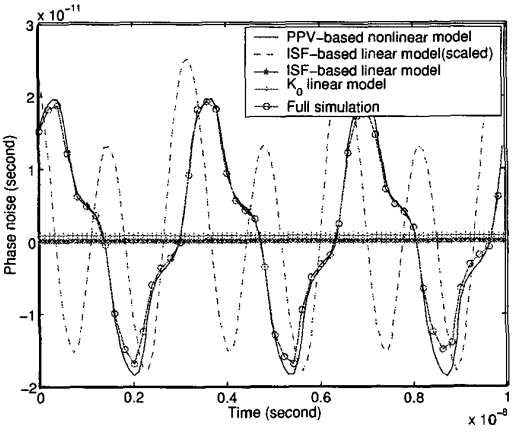


Fig. 6. The maximum phase nose due to the switching noise under different injecting time

the PPV and the noise perturbations. If the shape of the noise signal matches the PPV waveform well and provides a continuously growing slope, the PLL develops large phase errors and jitter. For example, Fig. 7(b) shows the waveforms of the PPV and periodic power supply noise with frequency $f = 3.03f_0$. The noise signal's shape matches the PPV well and always provides positive phase shift. So the PLL will experience large phase fluctuation if we inject a noise which is close to the PLL's third-order harmonic. Howerer, in Fig. 7(a), the noise signal's frequency is $1.01f_0$. The noise signal gives a positive phase shift in its first half cycle and a negative phase shift in its second half cycle. These two phase shifts cancel each other, so the PLL will have small phase fluctuation.

To verify our nonlinear phase macromodel, we first inject a sinusoidal signal with amplitude $A = 0.1mA$ and frequency $f = 3.03f_0$ to the power supply node and simulate the PLL for 100 cycles. The phase error of the PLL is shown in Fig. 8. The nonlinear phase model matches the full simulation very well. The sinusoidal noise signal generates a periodic phase shift to the PLL system. The maximum phase error is around 250ps, which is 2.5 percent of the PLL's period. The linear model does not work well in this case; it produces high frequency oscillations with very small amplitudes. The ISF macromodel still produces very small timing jitter under the same inputs. For comparison purpose, we scale the ISF waveform for a best match. Due to the nonlinear effect, the negtive part of the frequency sensitivity waveform will be stretched and the positive part will be compressed; as a result, the jitter waveforms of nonlinear macromodel and full simulation have a negative DC value. The ISF



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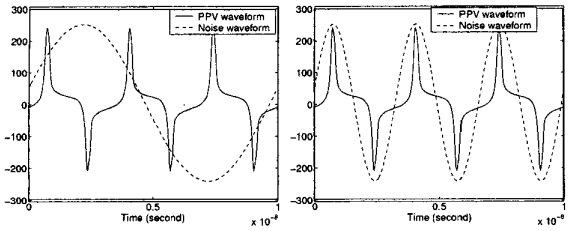


(a) (b)

Fig. 7. (a) The PPV and the power noise with the frequency $f = 1.01f_0$. (b) The PPV and the power noise with the frequency $f = 3.03f_0$.

model produces a balanced waveform in Fig. 8 as it is a linear model. We then apply a sinusoidal signal with amplitude $A = 0.1mA$ and frequency $f = 1.01f_0$ to the PLL. This time both nonlinear model and full simulation show the phase error of the PLL is less than 6ps.

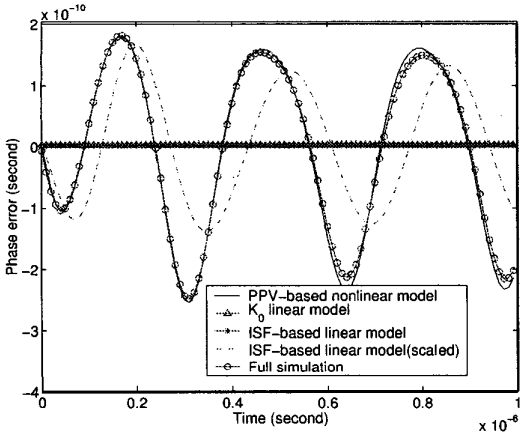


Fig. 8. The phase error due to supply noise with the frequency $f = 3.03f_0$

To fully reveal the relationship between noise frequency and phase error, we apply sinusoidal signals with different frequency to the PLL and plot the simulation results in Fig. 9. The frequency range in our tests is from $0.1f_0$ to $10f_0$, and the amplitude of the noise is fixed at $0.1mA$. Fig. 9 shows that the PLL experiences large phase error when noise frequency is close to the PLL's third-order or ninth-order harminic; otherwise, the phase error is very small. We also measure the phase error using full SPICE-level simulation, and the measurements show agreement between our nonlinear macromodel and full simulations. The ISF model produces very small phase deviations under the same inputs , so we have to scale it to match the full simulation. The jitter waveform of the ISF method has a peak on frequency $6f_0$, which is not existed in full simulation.

Using the nonlinear phase macromodel to simulate the PLL phase error gives us a dramatic speedup in simulation time. In sinusoidal noise simulation, the runtime using the full circuit simulation takes 1400 seconds for a simulation time of 100 cycles. However, it takes only 1.3 seconds to simulate the same number of cycles by using the nonlinear phase macromodel. This gives more than 1000 times speedup. Moreover, since the simulation time of the nonlinear macromodel does not increase significantly when the circuit size increases, speedups are expected to grow with larger VCO and PLL circuit blocks.

## V. Conclusions

We have presented an efficient nonlinear technique for predicting PLL jitter due to interference from supply grids. Our technique derives its accuracy from the fact that it captures the nonlinear impact of supply noise on jitter, while at the same time accounting *correctly* for the changing sensitivity of the oscillator during its oscillation cycle. We have tested he nonlinear phase macromodel using a ring-oscillator based PLL and provided detailed comparisons against full SPICE-level simulations as well as against prior linear jitter macromodels. Our numerical experiments show that the nonlinear macromodel is able to predict PLL jitter accurately even when prior linear techniques fail egregiously, while retaining large speedups over full SPICE-level simulation.

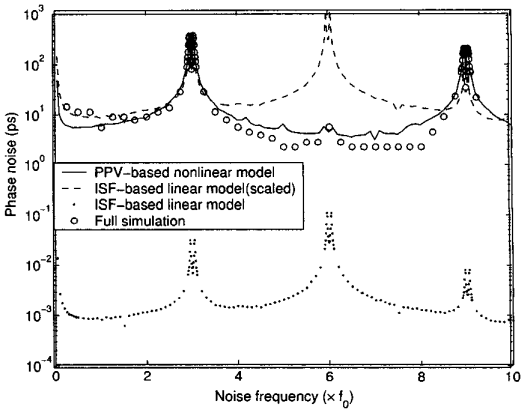


Fig. 9. The phase error due to sinusoid noise signal

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