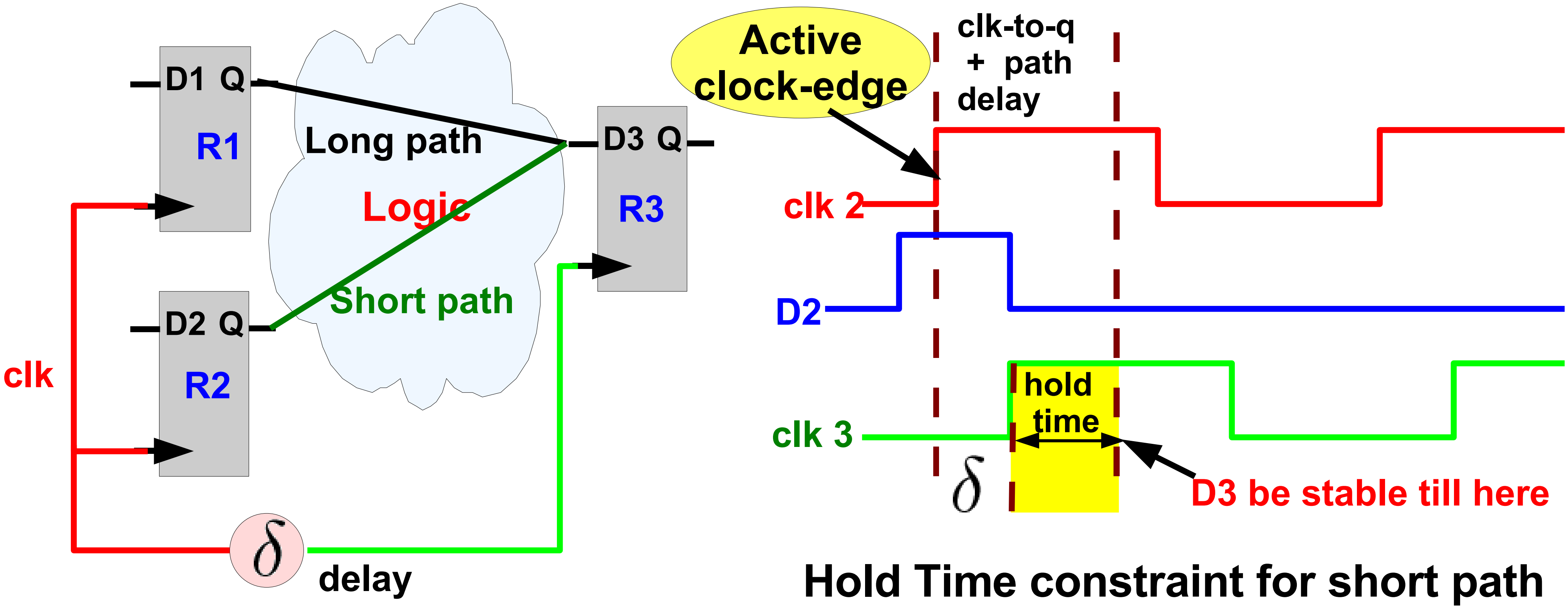
Interdependent Latch Setup/Hold Time Characterization via Euler-Newton Curve Tracing on State-Transition Equations

Shweta Srivastava, Jaijeet Roychowdhury

Dept of ECE, University of Minnesota, Twin Cities

shwetas@umn.edu

Setup/Hold Times in Timing Analysis



Hold Time constraint for short path

$$\text{hold-time}_{R3} + \delta < \text{clk-to-Q-delay}_{R2} + \text{short-path-delay}$$

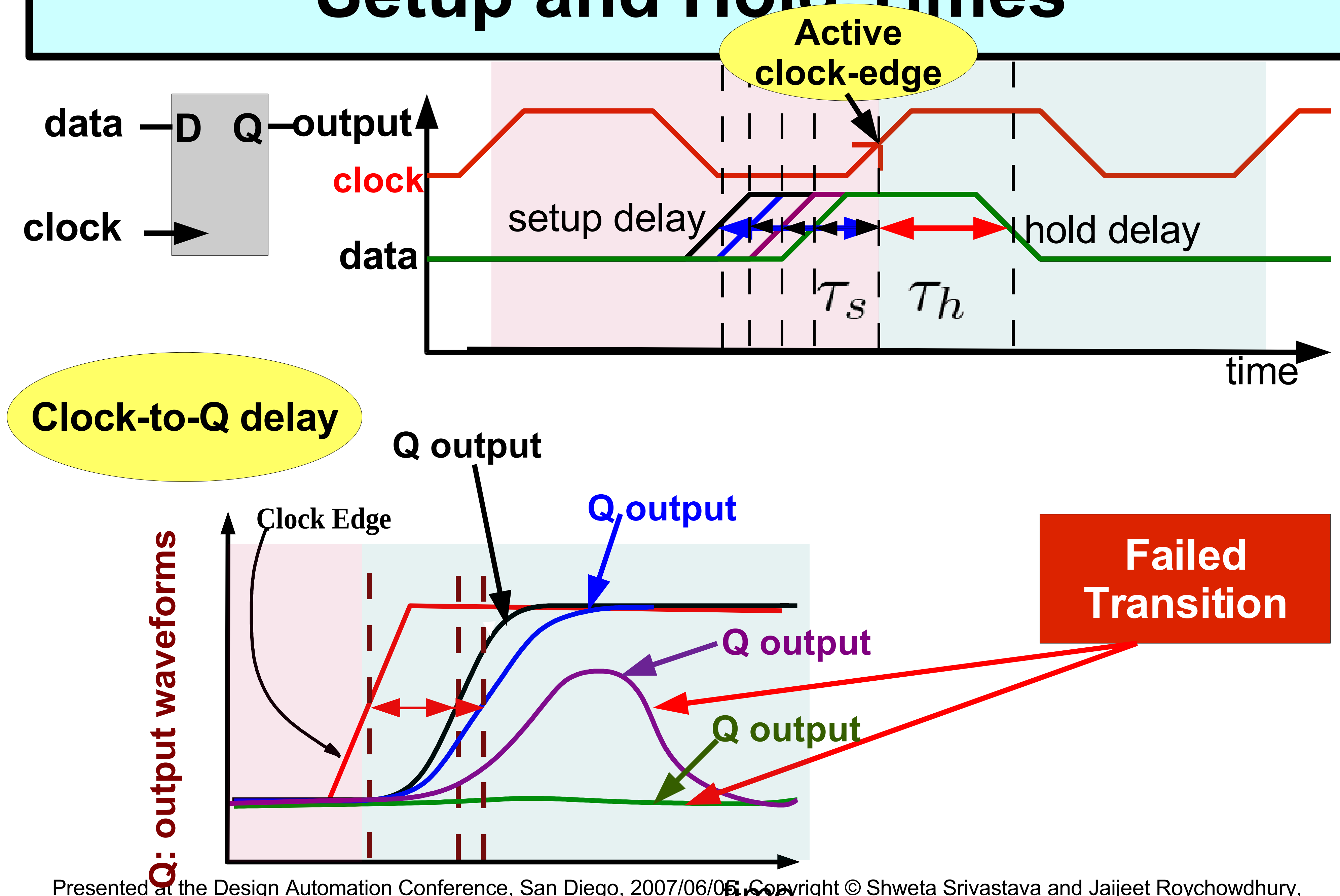
$$T > \text{clock-to-delay}_{R1} + \text{long-path-delay} + \text{setup-time}_{R3} - \delta$$

Setup/Hold Times: Important and Expensive

- **Finding setup/hold times**
  - Crucial component of library characterization
  - Accuracy all-important
    - detailed ckt level simulation, best models
  - Takes **months** for a cell library
    - Intel, IBM, AMD, ...

Finding setup/hold times is important but expensive

Setup and Hold Times



Is There Only ONE Setup and Hold Time?

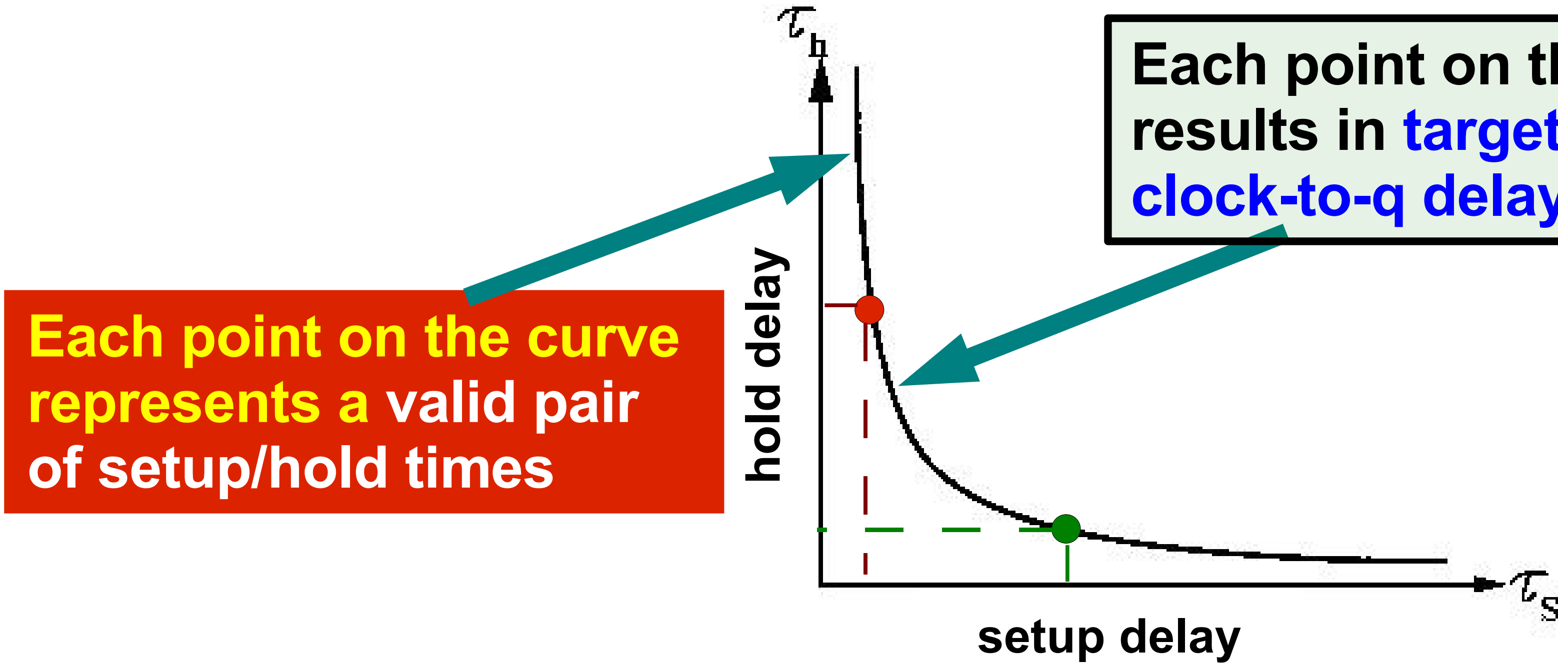
- **Assumption made today for STA:**
  - **setup/hold times unique**

Assumption NOT TRUE!

There can be many pairs of setup/hold times for a latch/register

Setup/Hold Time Tradeoff Curves

- E. Salman et al 2006 **(Ref [1] in paper)**

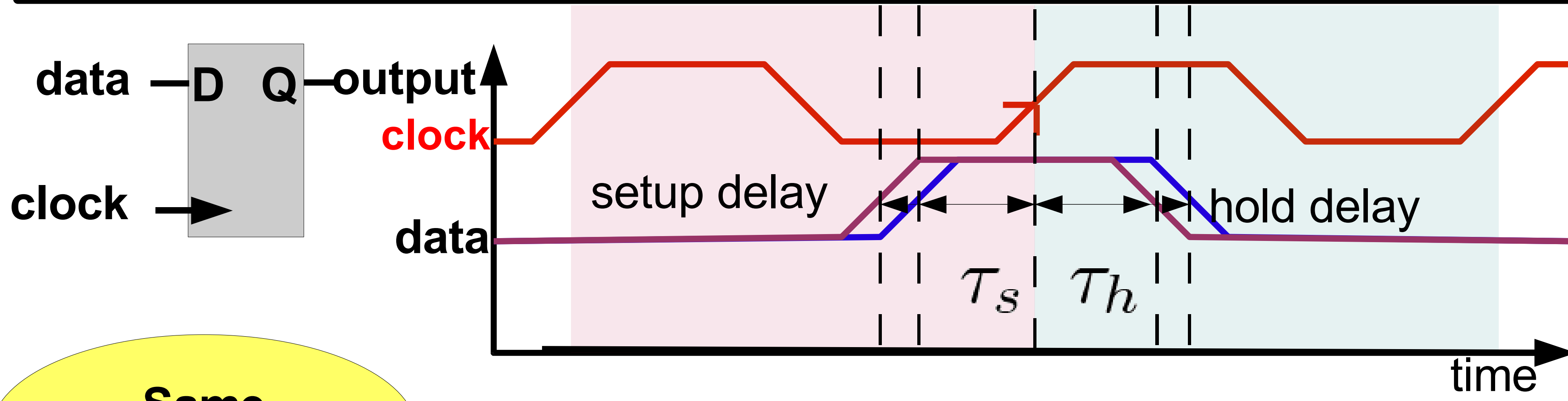


Setup/Hold Time Trade-off Curve

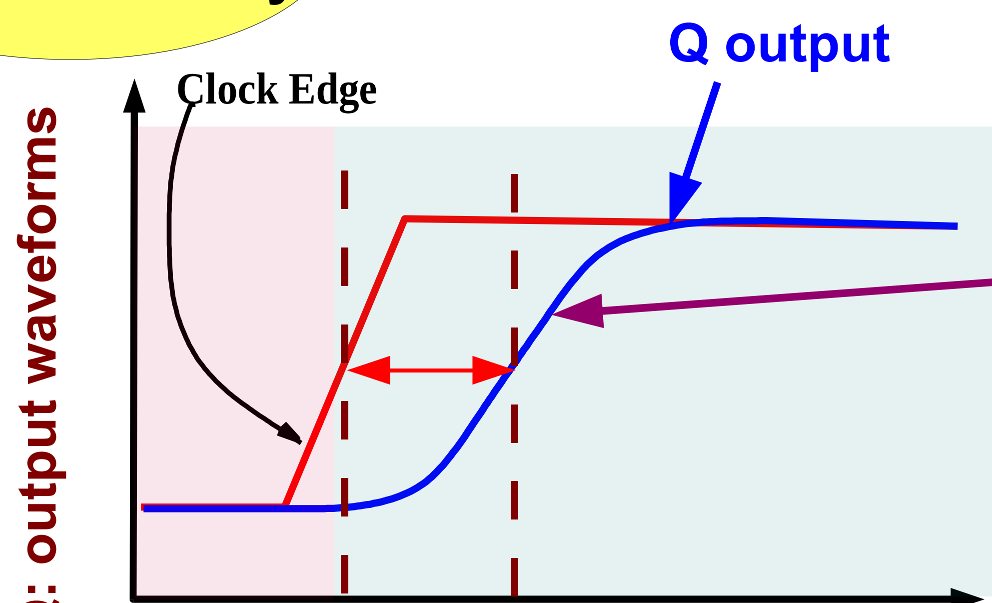
Impact

Reducing pessimism in timing analysis

Interdependent Setup and Hold Times



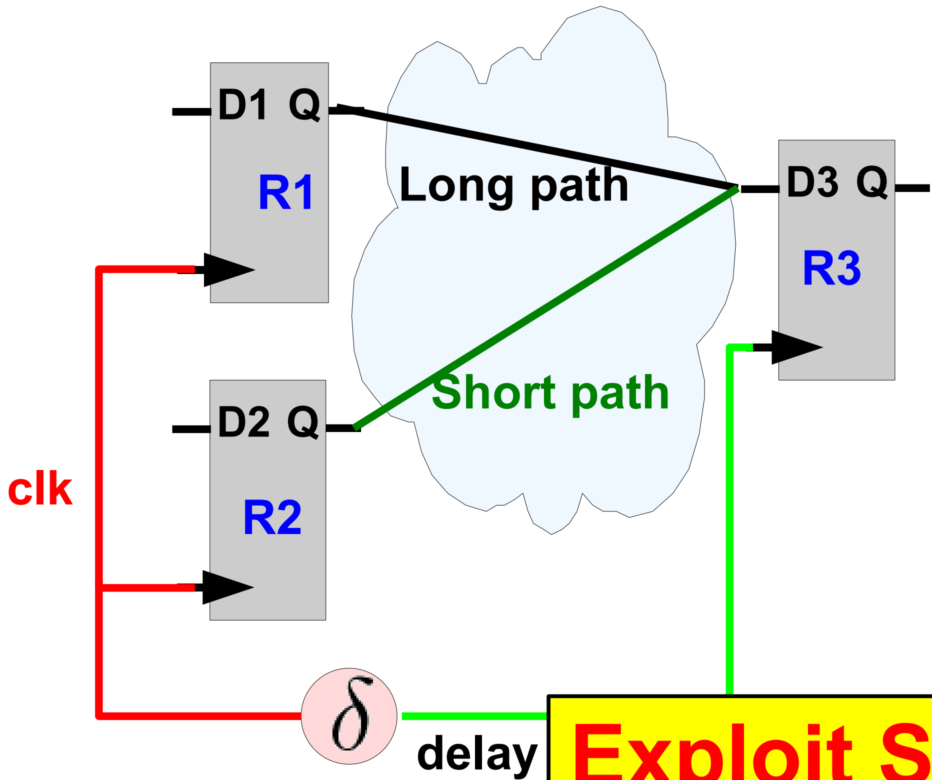
Same Clock-to-Q delay

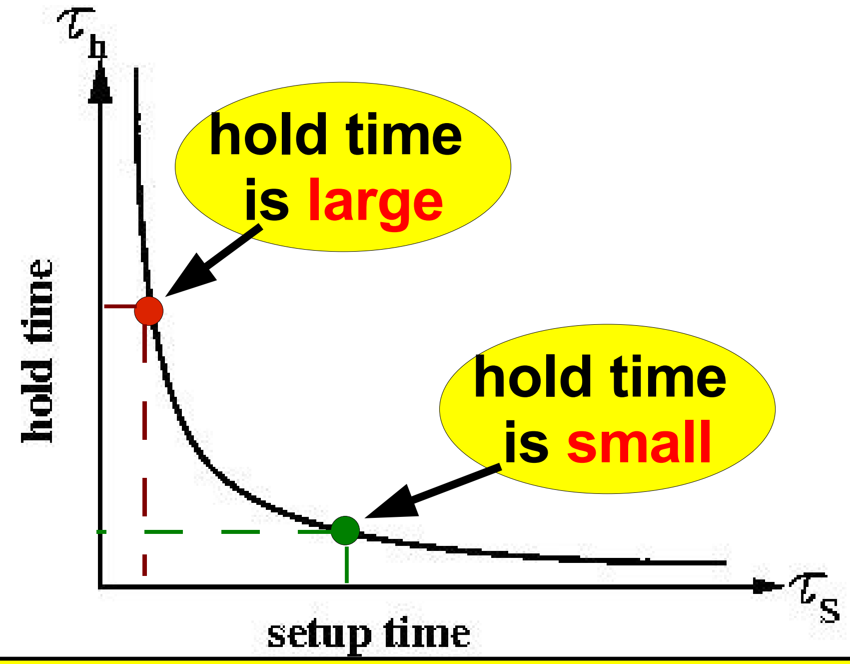


Same Q output

Same clock-to-Q delay for different setup and hold delays

How to Exploit Setup/Hold Interdependence in Timing Analysis?





Exploit Setup/Hold Time Trade-off

hold violation is removed

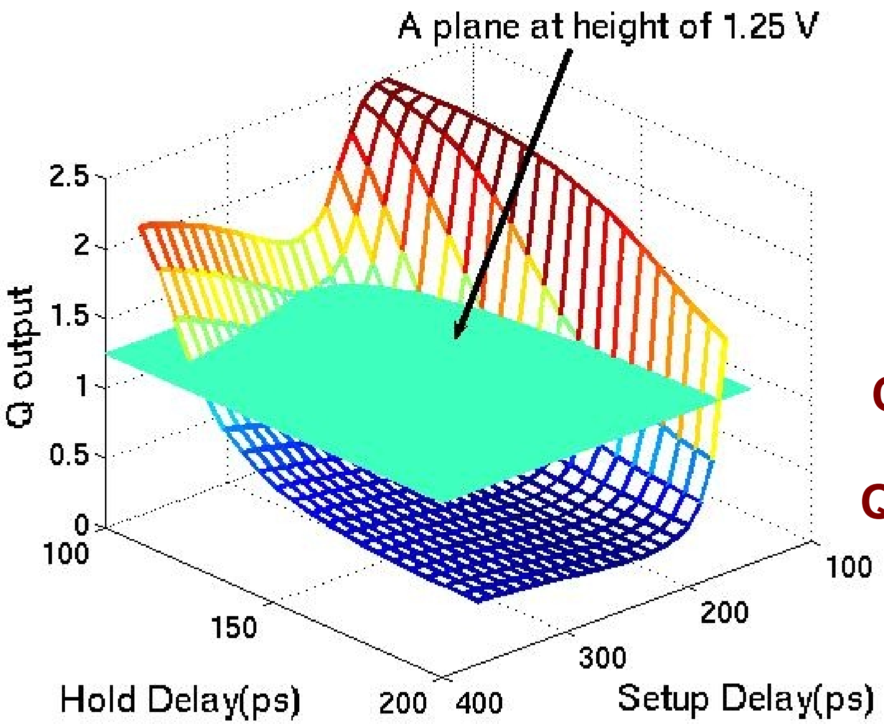
at the expense of larger setup time **may not be critical**

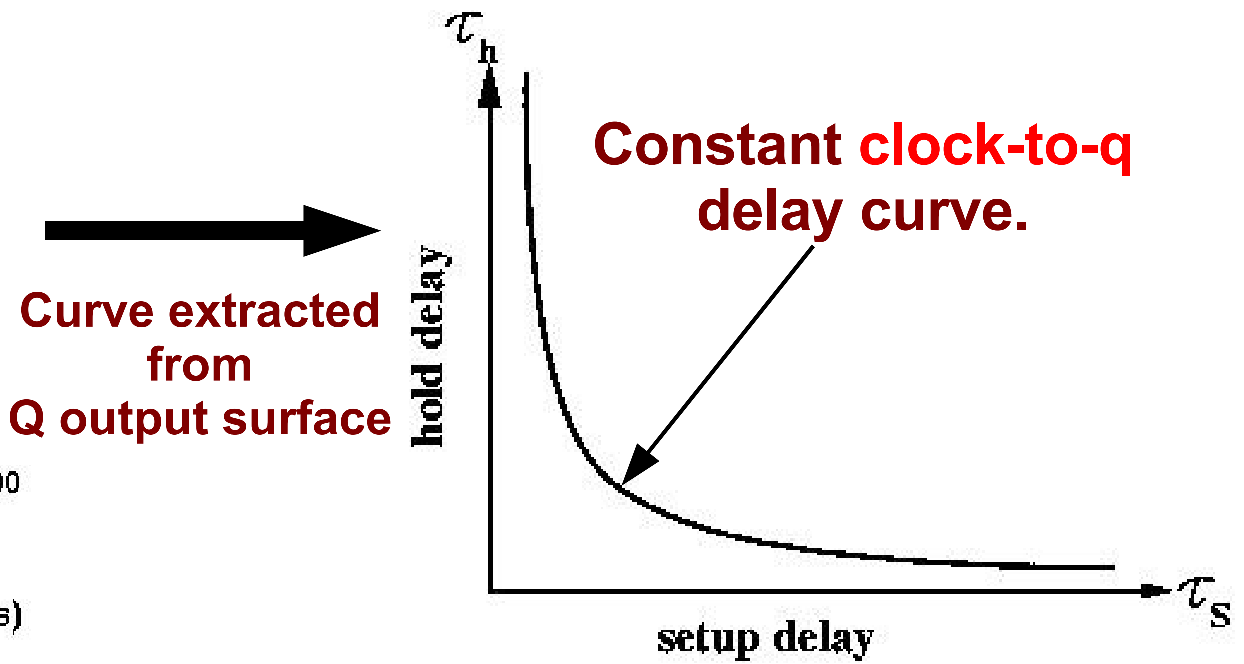
$$\text{hold-time}_{R3} + \delta < \text{clk-to-Q-delay}_{R2} + \text{short-path-delay}$$

Finding Tradeoff Curve is Very Important!

- Therefore:
  - Finding setup/hold tradeoff curve is very valuable
  - But:
    - <u>Very computationally expensive</u>

Why Expensive?





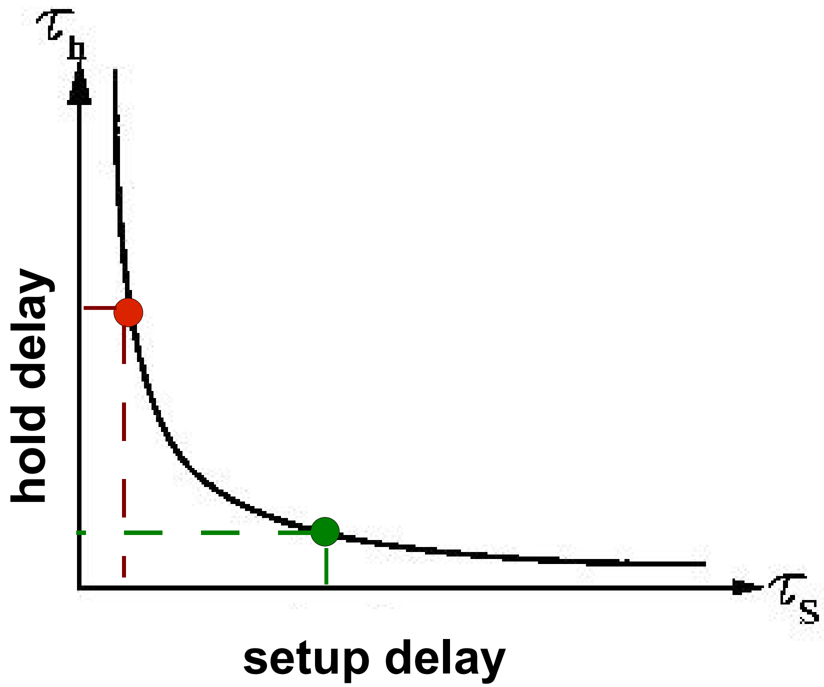
Q value vs setup and hold delays

- Problem: finding the full Q surface
  - Large number of transient simulations
  - i.e., infeasible in practice

Our Contribution: Find the Curve Quickly

- Contribution of this work
  - New setup/hold trade-off curve finding technique
  - much faster than prior brute-force technique
- Key idea: trace the curve "directly"
  - avoid looking at points far from curve

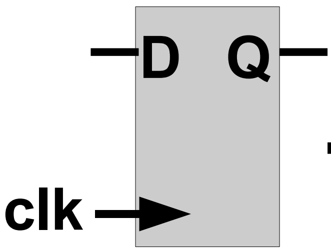
Our Formulation of the Problem



$$h(\tau_s, \tau_h) = 0$$

- A scalar equation with two unknowns (setup & hold time)
  - One equation, two unknowns => many solutions (the curve)
- Solve numerically using Newton-Raphson method
  - Rapid convergence

Formulation:



Differential equations for register

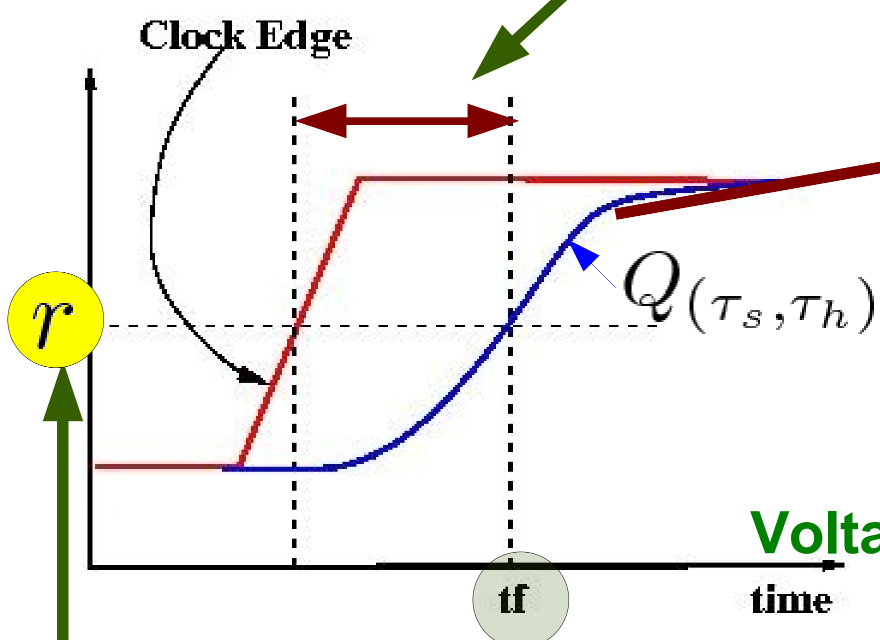
$$\frac{d}{dt}\vec{q}(\vec{x}) + \vec{f}(\vec{x}) + \vec{b}u(t) = 0$$

SPICE-level circuit

Target clock-to-Q delay

Q output waveform

$$Q_{t_f}(\tau_s, \tau_h) = r$$



setup time and hold time (unknowns)

Voltage threshold defining clock-to-Q delay

Contribution: Problem Formulation

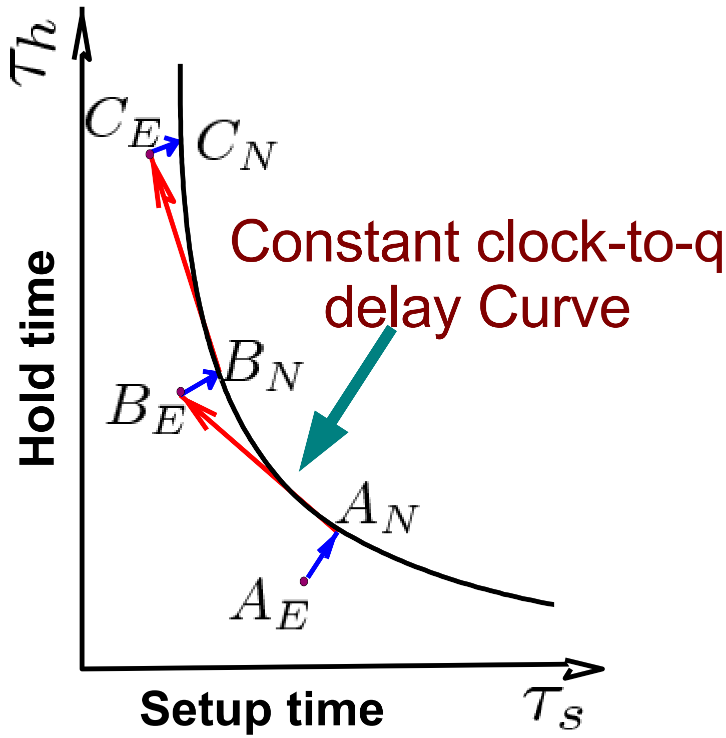
Q output waveform

$$Q_{t_f}(\tau_s, \tau_h) = r$$

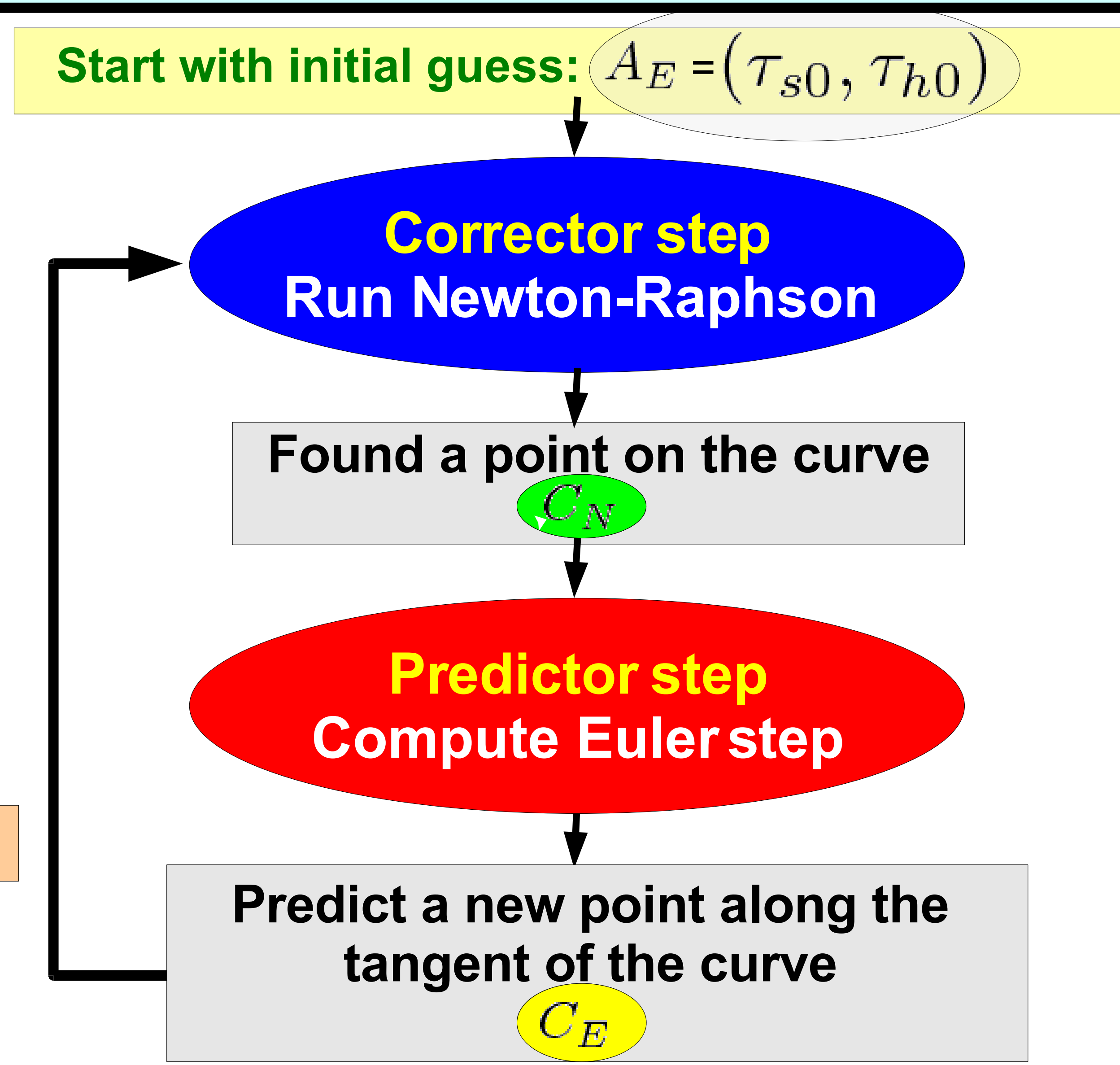
$$h(\tau_s, \tau_h) \equiv Q_{t_f}(\tau_s, \tau_h) - r = 0$$

- **Evaluation of $h(\tau_s, \tau_h)$ is a transient simulation**
- **Solution of ONE point**
  - **special type of Newton-Raphson (NR) method**
    - suitable for underdetermined equations
    - Moore-Penrose Pseudo Inverse NR (MPPI-NR)
- **Finding the entire curve**
  - **Euler-Newton** curve tracing method
  - Uses MPPI-NR for each point on curve

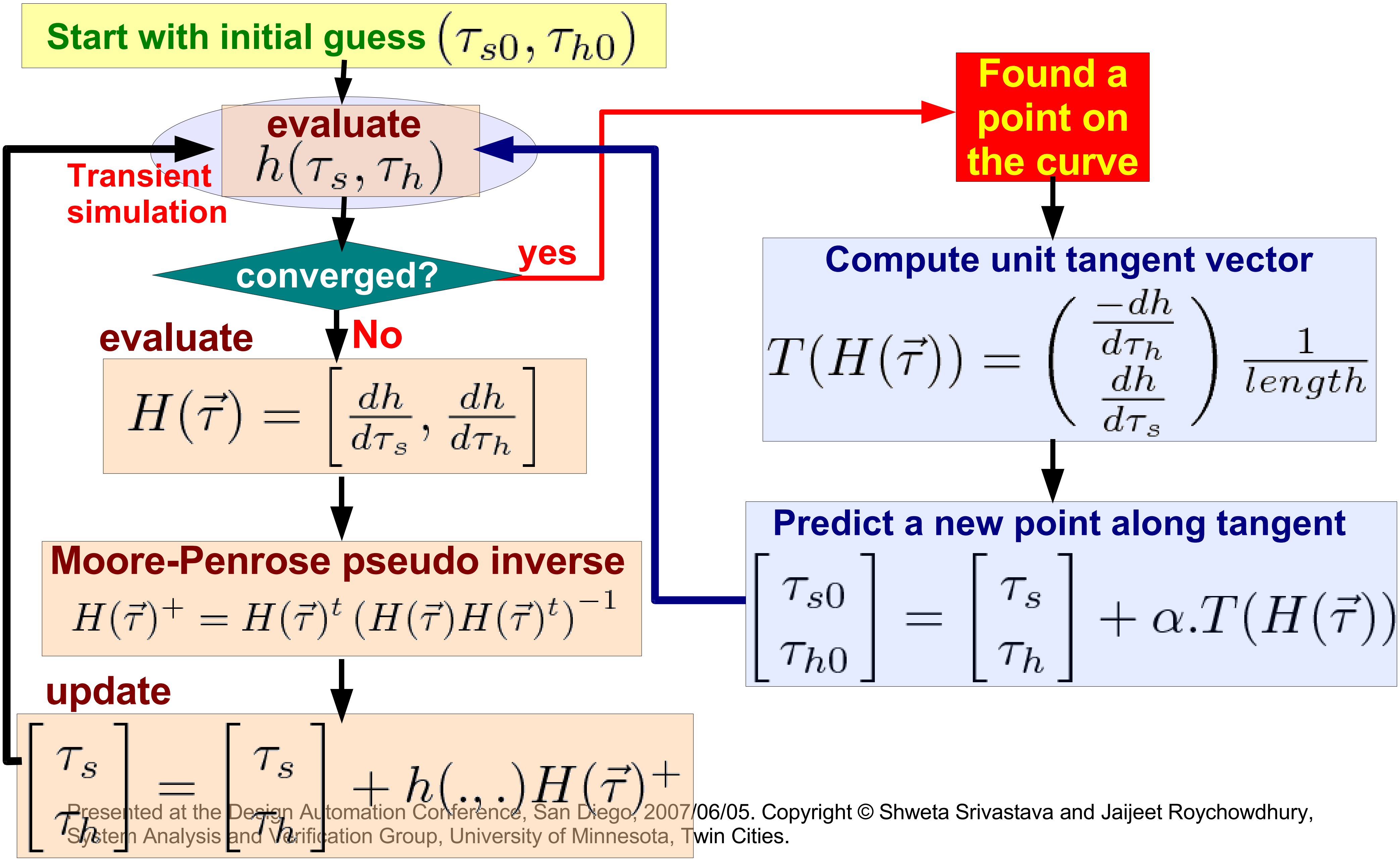
Intuition Behind Euler-Newton Method



Newton Step + **Euler Step**



Solving $h(\tau_s, \tau_h) = 0$ by Euler-Newton

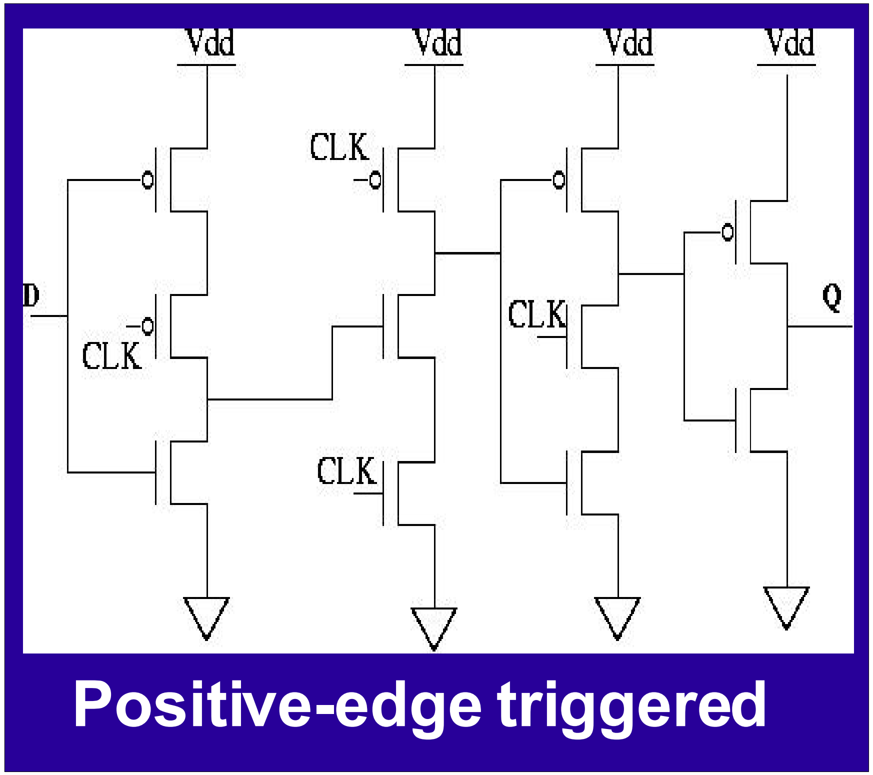


Connections with "RF" Simulation

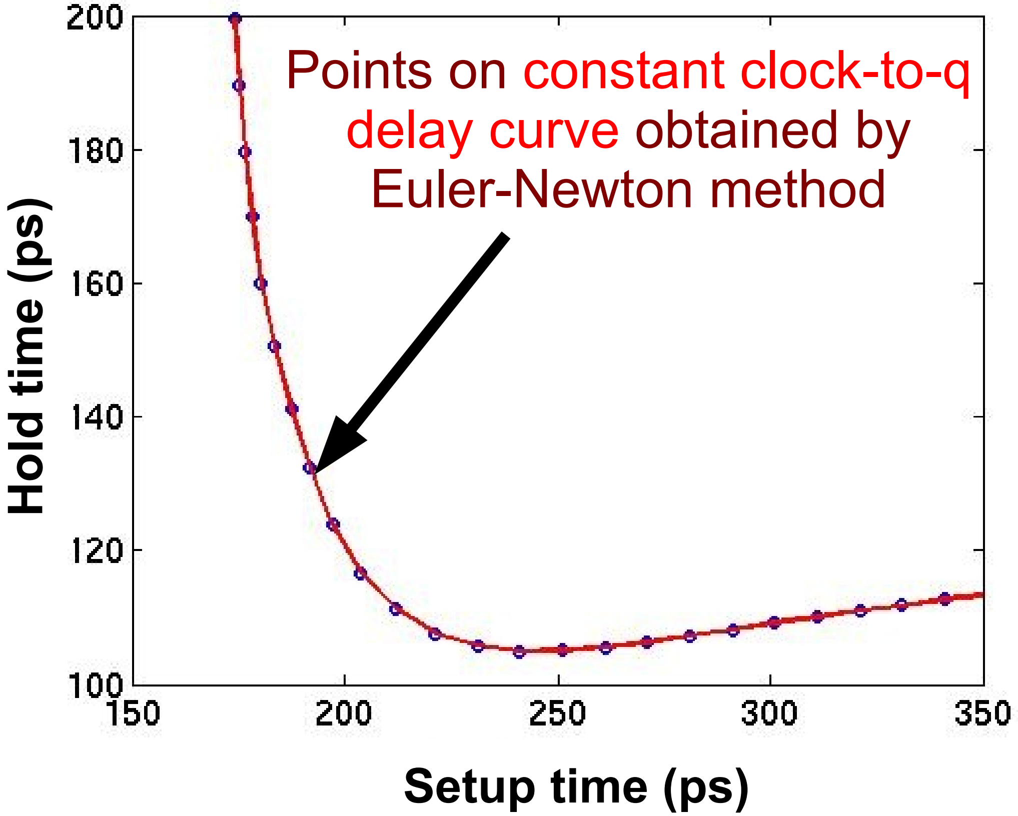
- **New Algorithm:**
  - **very similar to shooting method**
    - **used in "RF" simulation**
  - **Implementation easy in RF simulators**
    - Eg, **SPECTRE-RF (Cadence), MICA (Freescale)**
  - **"RF" simulation capabilities important for:**
    - **core characterization of digital circuits!**

Validation

Validation on TSPC register



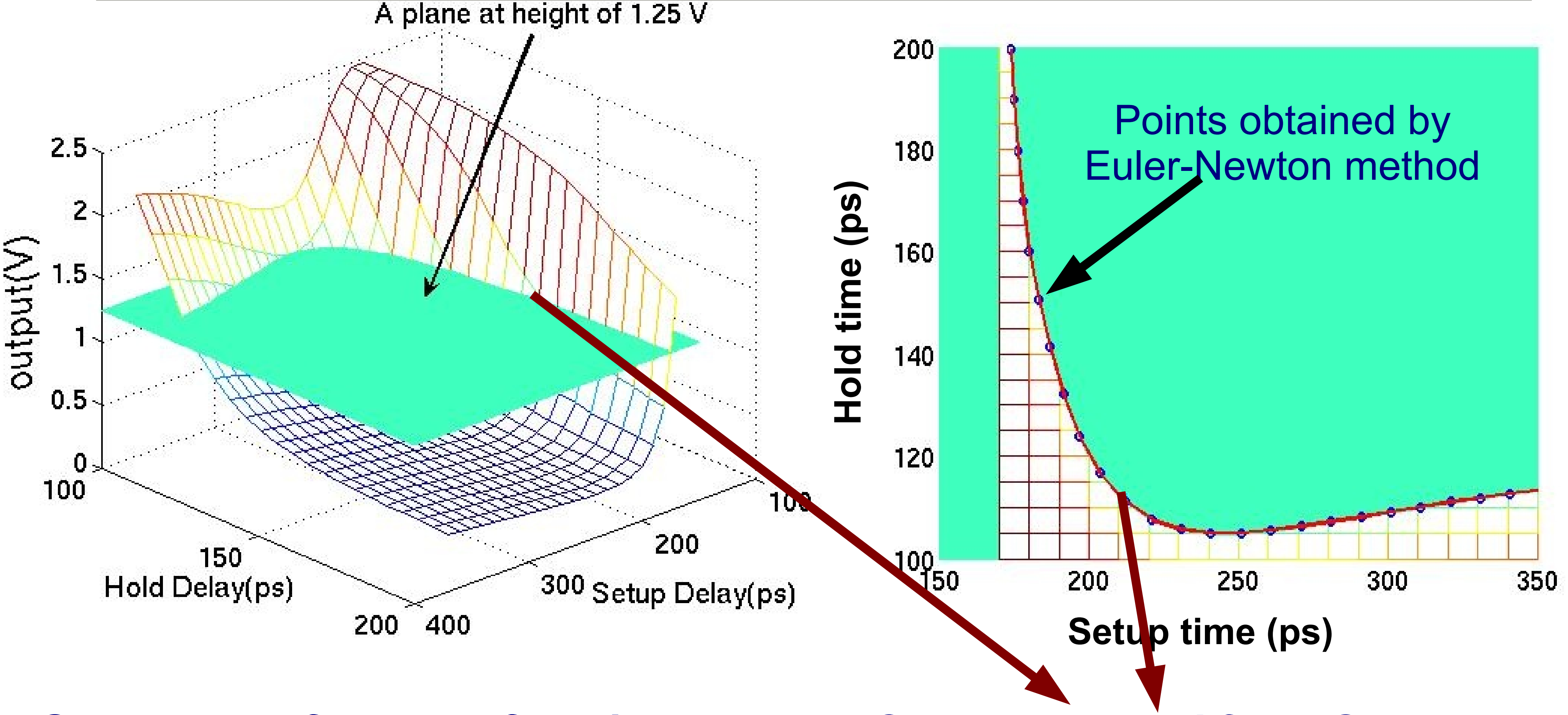
True Single-Phased Clocked register



Curve represents the pairs of setup and hold times – each point on curve results in 10% increase in nominal clock-to-Q delay

TSPC register validation

Speedup: ~12.5x (30min vs 6h 40min)

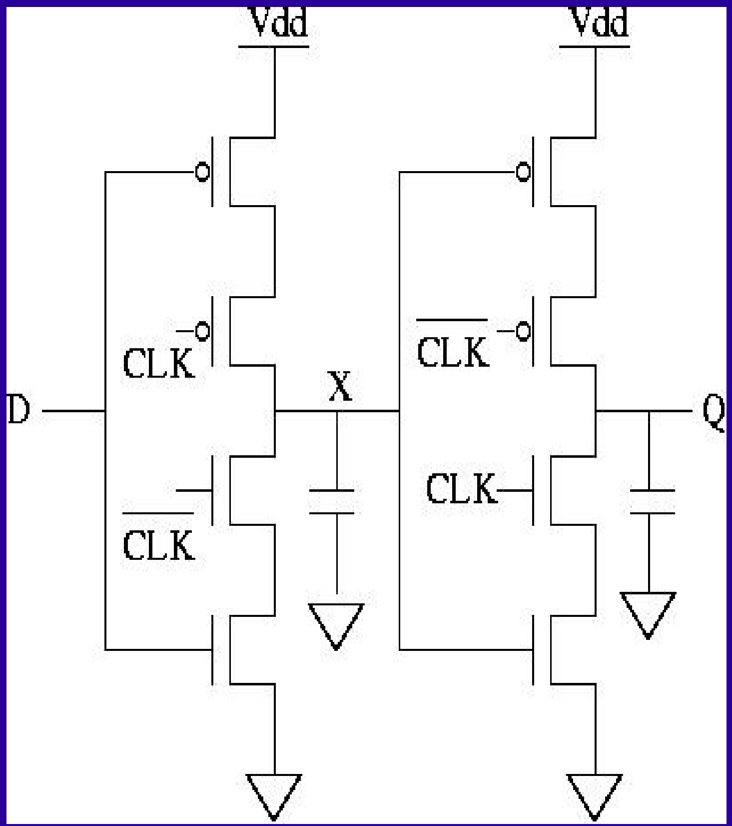


Q output surface as a function of setup and hold delays

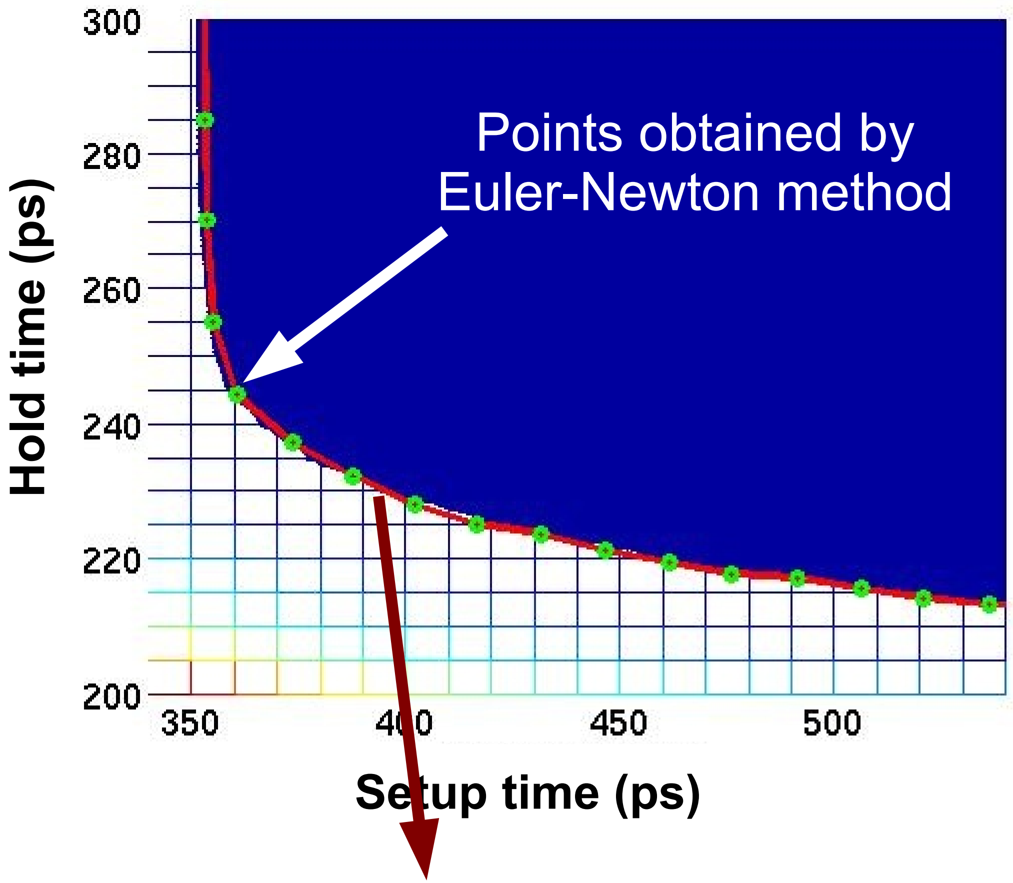
Curve extracted from Q output surface: Brute-force method

C^2MOS register: Validation

Speedup: ~10.5x (16min vs 2h 48min)



Positive -edge triggered



Curve extracted from Q output surface: Brute-force method

Summary

- **New technique for fast setup/hold tradeoff curve characterization**
  - **Adapts ideas from "RF" simulation (shooting)**
- Importance/Impact:
  - **"free" elimination of violations/slack in timing analysis**
  - **reduces unnecessary optimism or pessimism**
- **Validated on TSPC and C2MOS registers**
  - **Speedups of an order of magnitude**

Key advance in making setup/hold tradeoff exploitation

PRACTICAL

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