PHLOGON: PHase-based LOGic using Oscillatory Nano-systems

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Abstract. In this paper we take a fresh look at Goto and von Neumann's phase-based logic ideas, provide enhancements that can overcome major limitations of their previous implementations. We show that with injection locking serving as the central mechanism, almost any DC-powered, self-sustaining nonlinear oscillator — including electronic, spintronic, biological, optical and mechanical ones — can be used to build fundamental components — including latches and combinatorial elements in a phase logic based computing architecture. We also discuss noise immunity and potential power dissipation advantages that can be achieved under this scheme.

Keywords: Phase-based logic, nonlinear oscillators, injection locking.

1 Introduction

In the 1950s, Eiichi Goto and John von Neumann invented a new paradigm for computing: *temporal encoding* of logical states *using phases of oscillatory signals* [39,36,41,9]. Phase logic schemes corresponding to it have been implemented physically [13,28,27,35,25], indeed were popular in Japan in the 1950s due to their simplicity and reliability. However, the advent of transistors and integrated circuits led to their demise, since the devices and circuits they were based on could not compete with level-based logic using transistors.

A key reason for their lack of competitiveness was *size and miniaturizability*. Specifically, they normally require inductors and large capacitors, which are bulky compared to semiconductor transistors, particularly today's nano-scale MOS devices. Another related reason was *lower operating speed*, stemming not only from larger component sizes, but also from inherent features of von Neumann's scheme (*e.g.*, periodic turn-on transients and delays in logic gates) that made phase-based logic slower than transistorized level-based logic. Later attempts (from the 1980s to the present) used superconducting Josephson-junction devices [15], which are fast, but still limited in terms of miniaturizability and practical deployment at room temperature. Therefore, these implementations were quickly overshadowed by the rise of transistorized level-based logic, which has dominated logical computing for decades.

With power dissipation, variability and noise having emerged as serious barriers to semiconductor scaling and Moore's law — both synonymous with progress

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in computing — there has been renewed interest in Goto and von Neumann's phase-based logic ideas. Recently MEMS-based replacement for von Neumann's circuit has been proposed [21]. It could perform bit storage and bit flip operations under AC power and its success in implementing computation and large-scale integration is yet to be seen. In this paper, we propose enhancements (collectively termed **PHLOGON**) to Goto and von Neumann's schemes that employ *self-sustaining oscillators as basic phase logic elements* to eliminate the size and integrability limitations of the previous implementations, opening possibilities for robust, general-purpose computing substrates that offer *significant noise immunity and potential power dissipation advantages* over level-based CMOS computing.

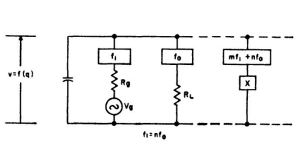
We describe how the core computational block — a finite-state machine (FSM) can be built using phase-based logic. As an example, we show how it can be realized using *CMOS ring oscillators in standard existing technologies*. However, PHLOGON is not limited to electronic oscillators. Indeed, it can use almost any self-sustaining nonlinear oscillator — including spintronic, biological, optical and mechanical ones – as the underlying logical element, expanding the implementation scope of Goto and von Neumann's phase logic ideas greatly.

To better explain our ideas, we provide background on Goto and von Neumann's phase-based computing scheme by summarizing von Neumann's related works in Sec. 2. In Sec. 3.1 we illustrate how sub-harmonic injection locking leads to multiple stable phase states, serving as the key mechanism for encoding phase logic. We show that phase logic offers inherently greater immunity to noise, interference and variability (Sec. 3.2). We then describe our implementation of phase-based computing architecture using self-sustaining nonlinear oscillators (Sec. 3.3) and discuss its potentially lower power/energy operation compared with traditional level-based CMOS computing scheme (Sec. 3.4). Conclusions are provided in Sec. 4.

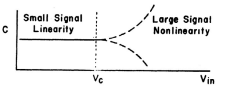
2 John von Neumann's Phase Logic Scheme

In his patent [39,36,41], von Neumann outlined fundamental ideas and a complete scheme for phase-based computing. We provide a brief sketch of the main ideas here.

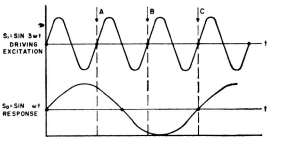
von Neumann started with a key observation: the circuit in Fig. 1(a) can feature *two (or more) distinct oscillating steady states*, which can be used to *store two (or more) logical states* stably. The circuit features a *lossless, nonlinear, charge-controlled capacitor* (shown towards the left of Fig. 1(a)), together with bandpass filters used to isolate an AC power source or *pump* (V_g), and an output load (R_L), from the several frequencies simultaneously present in the capacitor's terminal voltage. When the amplitude of the AC pump voltage waveform, assumed sinusoidal at frequency f_0, is larger than a critical threshold V_c (Fig. 1(b)), the voltage waveform across the capacitor can feature components that are *integer sub-multiples* of f_0, *i.e.*, *sub-harmonics of* f_0. Furthermore, as depicted in Fig. 1(c), a generated sub-harmonic can be in *one of several distinct*



(a) AC-powered subharmonic generator features multiple phase-shifted stable states [41, Fig. 2].



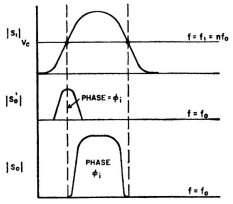
(b) Multistability beyond a critical pump amplitude, V_c [41, Fig. 4].



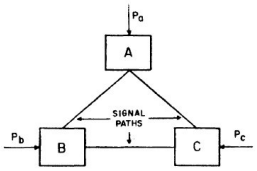
(c) Example: discriminating between subharmonic steady states [41, Fig. 6].

Fig. 1. von Neumann's basic phase-based latch: a nonlinear AC-pumped circuit with multiple subharmonic steady states

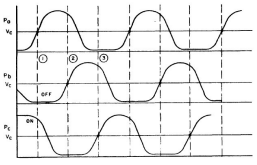
phase relationships with respect to the waveform of the AC pump. Each distinct phase relationship can be used to encode a logic state. The circuit functions, effectively, as a *latch* that can store a logic value. The sub-harmonic and multistability properties of the circuit in Fig. 1(a) can be inferred from an elegant formula, the *Manley-Rowe relationships* [39,23,41].



(a) Amplitude modulation of the AC pump to capture an input logic value [41, Fig. 7].



(b) A ring of latches can retain a phase-logic state permanently [41, Fig. 11].



(c) Phase-shifted amplitude modulation waveforms driving the ring of latches [41, Fig. 11].

Fig. 2. von Neumann's scheme for setting a latch to an input state and retaining it

Setting a phase-encoded latch to an input logic state: Having devised a latch circuit capable of storing logical values encoded in phase, von Neumann considered the question of setting a latch to a desired logic state supplied as input. He proposed a scheme based on modulating the amplitude of the AC pump slowly with a waveform similar to the uppermost graph of Fig. 2(a). When this modulation waveform is low, the latch is, effectively, turned off; as the modulation increases and magnitude of the AC pump crosses the critical threshold V_c, the latch turns on and settles to one of the possible logic states. von Neumann suggested that if a desired logic value (encoded in phase) were to be introduced as an input to the latch just as it was turning on, the latch would settle to (the sub-harmonic phase corresponding to) the same logic value. This is depicted in the middle and bottom graphs of Fig. 2(a).

Holding on to the logic state: A problem with the above input-latching scheme is, of course, that the latch is turned off periodically, thereby losing its stored

state. von Neumann's solution was a ring of latches (Fig. 2(b)), with each latch's AC pump modulated by a phase shifted version of its predecessor's AC modulation (Fig. 2(c)). The ring operates in merry-go-round fashion, with each succeeding latch turning on, capturing its predecessor's logic state and retaining it as the predecessor subsequently turns off. At any given time, one latch is always on, hence the logic state is never lost.

Combinatorial operations for phase-encoded logic: Next, von Neumann turned to the problem of realizing arbitrary Boolean operations using phase-encoded logic. Noting that two operations, NOT and MAJORITY, constitute a logically complete set [1], he provided especially elegant means of realizing them [41]. NOT is obtained simply by a through connection between latches with different pump modulation phases while MAJORITY is obtained simply by adding the waveforms of the three inputs together.

Having devised phase-based realizations of the latch-ring and the logically complete combinatorial function set NOT and MAJORITY, together with a consistent timing scheme provided by the phase shifted pump modulation waveforms, von Neumann had developed all the basic components needed to make state machines and general computing architectures.

3 PHLOGON: Key Concepts

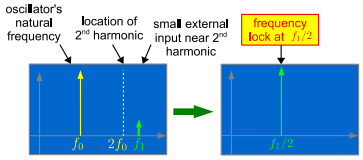
As discussed before in Sec. 1, previous implementations of von Neumann's scheme suffer from limitations and have not, to date, been miniaturisable or large-scale integrable. In this section, we detail our ideas for PHLOGON, explain their novelty and significance.

3.1 Sub-harmonic Injection Locking (SHIL) Enables Phase Logic

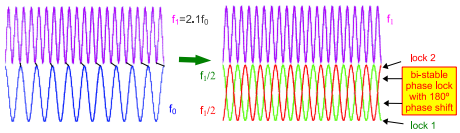
A central paradigm in PHLOGON is that DC-powered nonlinear self-sustaining oscillators can be used as phase logic elements. This paradigm relies on the fact that such oscillators inherently feature a property known as *injection locking* [16,2,19], which enables the oscillator's waveforms to move in lock-step with – *i.e.*, become *phase locked* to – a small external signal injected into it[2]. Injection locking is responsible for many *sychronization phenomena* in nature (*e.g.*, the synchronized flashing of fireflies [4,34,33]) and is exploited in engineering (*e.g.*, injection locked frequency dividers [30]).

A specific type of injection locking, known as sub-harmonic injection locking (SHIL), is the key mechanism involved in phase logic encoding. We have developed theory that shows how SHIL leads to multiple stable phase states[1], as depicted in Fig. 3(b). We have also been able to distill the essential properties needed in an oscillator for it to be an effective sub-harmonically locked oscillator-latch. We provide a sketch of our ideas and results here.

[1] *i.e.*, any Boolean function can be realized using compositions of functions in this set.
[2] Phase locking also ensures that the frequency of the oscillator becomes identical to that of the input.



(a) When SHIL happens, the oscillator's frequency locks to the sub-harmonic of the input.



(b) When SHIL happens, phase lock features multi-stability. In this case where $f_1 \approx 2f_0$, there are two stable states with 180° phase difference.

Fig. 3. Illustration of frequency and phase lock of sub-harmonic injection locking

The phase response of any amplitude-stable nonlinear oscillator to small external inputs can be captured via a so-called Phase Response Curve (PRC) [22,42,17] or Perturbation Projection Vector (PPV) [7] equation as in (1).

$$\frac{d}{dt}\alpha(t) = \boldsymbol{v}_1^T(t + \alpha(t)) \cdot \boldsymbol{b}(t). \tag{1}$$

In (1), $\alpha(t)$ is a changing *time shift* or *jitter* in the oscillator's waveform caused by $\boldsymbol{b}(t)$, containing small inputs to the oscillator. $\alpha(t)$ is related very simply to the phase shift to the oscillator's response.

The importance of the PPV equation[3] (1) for oscillator-latches lies in that it can model and predict injection locking effectively [20]; however, though easily solved using numerical methods, analytical solution of (1) is usually not possible. To obtain insights into injection-locking properties, and for visualisation and design, we have developed a simplified approximation of (1) known as the *Generalized Adler Equation* (GAE) [3,2]. Given specific periodic inputs to the oscillator, the GAE governs the dynamics of the oscillator's phase as it evolves; in particular, the equilibrium states of the GAE provide good approximations to injection-locked solutions of the PPV equation (1).

Suppose that the PPV of an oscillator-latch consists of a fundamental sinusoidal component (at the oscillator's natural frequency, f_0) of strength k_1, plus a second harmonic component of strength k_2. For the oscillator to develop multi stable phase states, we apply a small input SYNC of amplitude A_1 at frequency $f_1 \simeq 2f_0$[4]. With SHIL, the oscillator changes its frequency to $f_2 \triangleq \frac{f_1}{2}$ (Fig. 3(a)) and its phase becomes bi-stable (Fig. 3(b)). To control which stable phase the oscillator will latch, we apply another input of amplitude A_2 at frequency f_2, with phase shift (relative to SYNC) θ[5]. This input corresponds to one of the stable states thus can be encoded to have a logic value (0 or 1 in binary

[3] Well-established computational techniques are available [8,7] to obtain the quantity $\boldsymbol{v}_1^T(\cdot)$, known as the PPV or PRC, of any nonlinear oscillator described in differential equations.

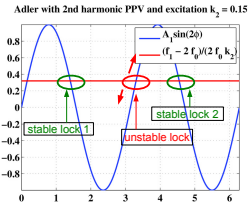
[4] We have shown that when SYNC is at $f_1 \simeq mf_0$, the phase of the oscillator may feature m distinct stable states and the analysis performed here is still applicable[3,1]. We will henceforth take $m = 2$ (binary encoding) to illustrate all the main ideas.

[5] $\theta = 0$ and $\theta = \pi$ correspond to the two logic states for binary phase logic.

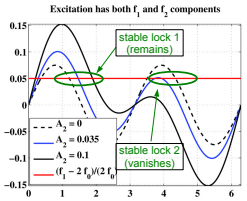
logic). We have shown that the GAE equilibrium equation corresponding to this situation is (2).

$$\frac{f_1 - 2f_0}{2f_0} = k_1 A_2 \sin(\phi - \theta) + k_2 A_1 \sin(2\phi)\,. \tag{2}$$

Solutions ϕ of (2) are the possible phase shifts of the oscillator-latch's waveforms when it is sub-harmonically injection locked. Considerable insight into the number, nature and behaviour of these solutions can be obtained graphically, by plotting its left- and right-hand-sides separately and looking for intersection points.



(a) (2) has 2 stable solutions in the absence of a (logic) input.



(b) Acquisition of input phase: phase bistability of (2) vanishes.

Fig. 4. GAE equilibrium equation (2) establishes multi-stability and input phase acquisition properties of oscillator-latches

Fig. 4(a) plots the left- and right-hand-sides (flat red and sinusoidal blue traces, respectively) of (2) when $A_2 = 0$ and no logic input is present at the oscillator-latch. There are 4 intersections between the two traces, corresponding to 4 solutions of (2). Of these, the first and third intersections (from the left) can be shown to be dynamically unstable[6]; but the second and fourth intersections correspond to *two distinct stable oscillations, sub-harmonically locked to* SYNC *with phases separated by* π *radians*. Thus, in the presence of SYNC, the oscillator-latch features bi-stability.

Fig. 4(b) plots the same left-hand-side (flat red trace), but overlays several traces for the right-hand-side of (2), corresponding to A_2 values 0, 0.035 and 0.1, with the latter two values representing two different strengths of an incoming logical signal at f_2 with $\theta = 0$. As can be seen, the first stable intersection remains relatively unaffected as the strength of the incoming input changes, but the second intersection vanishes, structurally, for A_2 value 0.1. This implies that the oscillator acquires the input's logic state. After acquisition, as A_2 is reduced to zero, the GAE can be used to analyze the dynamics of ϕ and show that the acquired logic state is held, even though the second stable intersection is restored.

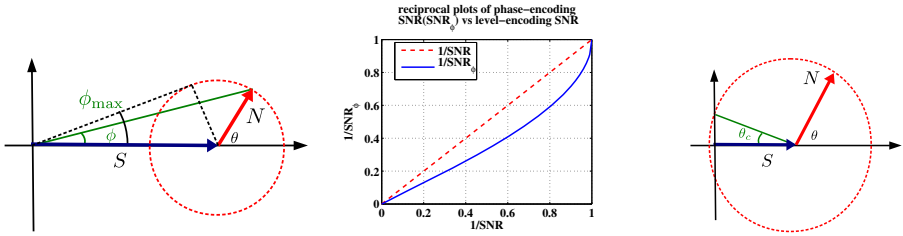
In summary, the SHIL phenomenon enables the oscillator to develop multiple, well-defined, stable states that can be used to encode logic. It also shows how

[6] *i.e.*, they are physically unrealizable in the presence of perturbations, noise or variability.

the oscillator-latch can acquire phase and switch between logic states according to external logic inputs.

3.2 Inherent Noise Immunity of Phase-Based Logic

One of the key attractions of encoding logic in the phase of oscillatory signals is that, compared to level-based schemes, phase encoding provides inherent resistance to errors caused by additive noise and interference. There are two aspects to phase encoding that provide intrinsic resistance to additive noise/interference: 1) the effective SNR[7] for phase is increased by a factor of $\frac{\pi}{2}$ over SNR for level-based encodings, and 2) the oscillatory nature of the signal whose phase encodes the information makes much of the additive noise/interference average out, leading to smaller bit error rates than for the level-based case. These mechanisms are explained below.



(a) 1st mechanism: vector addition increases noise immunity in the phase domain.

(b) 1st mechanism: $\frac{1}{\text{"phase SNR"}}$ (blue) vs. $\frac{1}{\text{(level-based) SNR}}$ (red).

(c) 2nd immunity mechanism: averaging over θ reduces bit error rate.

Fig. 5. Mechanisms enhancing the noise resistance of phase-encoded logic

Fig. 5(a) depicts an oscillatory signal as a phasor [12] $\boldsymbol{S}$, superimposed upon which is a noise (or interference) component, $\boldsymbol{N}$. The impact of this noise on the phase of the signal is shown by the phase error $\phi = \angle(\boldsymbol{S} + \boldsymbol{N})$. Given fixed amplitudes[8] $S = |\boldsymbol{S}|$ and $N = |\boldsymbol{N}|$, ϕ depends on the relative angle θ between $\boldsymbol{S}$ and $\boldsymbol{N}$, *i.e.*, $\phi = g(\theta, \frac{N}{S})$[9]. For $N < S$ and fixed N/S, there is a maximum phase error over all θ, *i.e.*, $\phi_{\max} = \sin^{-1}(N/S)$, as depicted in Fig. 5(a). The "phase SNR" is given by $\text{SNR}_\phi = \frac{\frac{\pi}{2}}{\phi_{\max}}$; it is the fraction, in angular terms, of the first quadrant taken up by the maximum phase error. This is to be compared against S/N, the SNR for level-based logic (for which, in Fig. 5(a), $\boldsymbol{N}$ is collinear with $\boldsymbol{S}$). As can be seen from Fig. 5(b), $\frac{1}{\text{SNR}_\phi}$ is always smaller than $\frac{1}{\text{SNR}}$, *i.e.*, the "phase SNR" is always improved over the standard level-based SNR. For small S/N (*i.e.*, a large level-based SNR), this improvement is a factor of $\frac{\pi}{2} \simeq 1.6$. This is the first mechanism by which phase encoding improves noise immunity.

[7] Signal to noise ratio.

[8] For illustrative simplicity, we consider noise of only a fixed magnitude. In reality, of course, the magnitude of $\boldsymbol{N}$ has a probability distribution, *e.g.*, a Gaussian one.

[9] For example, $g(0, \cdot) = g(\pi \cdot) = 0$ and $g(\frac{pi}{2}, \frac{N}{S}) = \tan^{-1}(\frac{N}{S})$.

A second mechanism, conferring additional noise immunity, stems from that the phasors $\boldsymbol{S}$ and $\boldsymbol{N}$ are not necessarily always at the same frequency (as assumed implicitly in the analysis of the first mechanism, above), but can rotate at different speeds[10]. Consider now the case where the rotation speeds are very different. The rapid relative change in the angle θ between $\boldsymbol{S}$ and $\boldsymbol{N}$ suggests that the worst-case phase error $\phi_{\max}$, from the first mechanism above, is unduly pessimistic; and that, instead, the phase error *averaged over all values of* θ is the appropriate measure. More precisely, the standard deviation σ_ϕ that results from, *e.g.*, uniformly distributed θ, is an appropriate measure of the phase error. This quantity can be substantially smaller than the worst-case phase error $\phi_{\max}$, implying considerable additional immunity to noise.

Indeed, this second mechanism makes phase encoding useful even when the noise magnitude is *greater* than that of the signal, a situation where level-based logic encoding becomes largely useless. This situation is illustrated in Fig. 5(c). Observe that for most values of θ, the phase error is less than $\frac{\pi}{2}$, the threshold for a bit error. The probability of logical error in the case of phase encoding is $\frac{\theta_c}{\pi} = \frac{\cos^{-1}(S/N)}{\pi}$, which can be very small if N is only slightly greater than S (as depicted); and reaches its maximum, 50%, only as the noise increases to infinity. In contrast, the probability of logical error for level-based encoding is always 50% when $N > S$, since a logical error *always* results when the noise subtracts from the signal (rather than adding to it).

These noise immunity features of phase encoding do not come as a surprise; the superior noise properties of phase and frequency modulation (PM and FM), over those of amplitude modulation (AM), have long been known [24] and exploited in practice, *e.g.*, in radio communications. However, the authors are not aware of their prior realization, or application, in the context of logic encoding for general-purpose computing.

3.3 Computation with Phase Logic

With phase-based logic encoding, we describe ideas on the implementation of phase-based computing in this section.

The central unit of a computer is a finite-state machine (FSM) [36]. As is shown in Fig. 6, latches and combinational logic blocks are the key components of an FSM. We first describe how to build combinational logic blocks using phase logic.

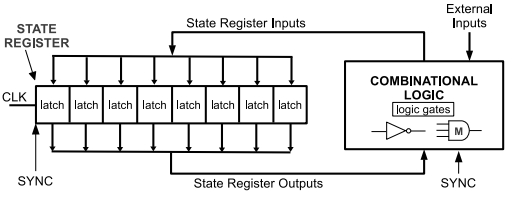
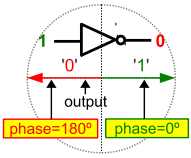


Fig. 6. A general FSM. SYNC is used to develop multi-stability for encoding phase logic; NOT/MAJORITY gates are for combinatorial operations.

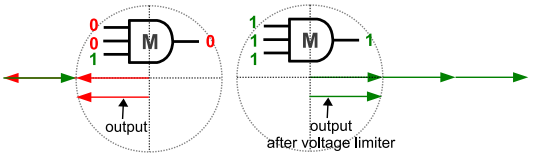
We realize combinatorial operations in a manner almost identical to von Neumann's technique,

[10] The phasor $\boldsymbol{N}$ can be thought of as one component, at frequency f, of a spectral expansion [14] of a stochastic process.

using NOT and MAJORITY operations. Phase logic enables elegant implementation of these two operations: NOT is simply inversion and MAJORITY can be implemented by addition. These can be explained using phasors, as is demonstrated in Fig. 7.



(a) Inverting input signal performs NOT operation in phase logic.

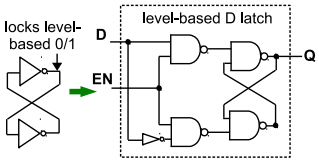


(b) A three-input MAJORITY gate uses addition to perform MAJORITY operation of input signals in phase logic.

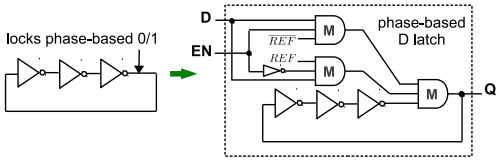
Fig. 7. Phase-domain plots illustrating NOT and MAJORITY operations

With oscillator-latches to store phase-based bits and logic gates to perform combinatorial operations, we now have all the components to build general-purpose computing systems using phase logic. Without loss of generality, here we use CMOS ring oscillators as an example to show how such computing systems can be built.

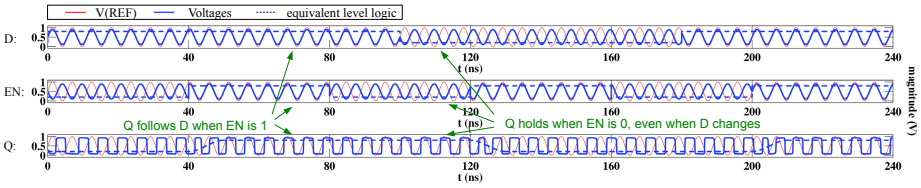
Fig. 8(b) shows a diagram of a D latch implemented using phase logic. The design is analogous to that of a level-based D latch (Fig. 8(a)) except that information is latched in phase. Fig. 8(c) shows waveforms from SPICE-level simulation of the implementation of phase-based D latch with ring oscillators. By aligning the waveforms of Q, D, EN with REF, we see that it achieves the functionality of a transparent D latch in phase logic.



(a) Level-based D latch derives from bi-stable level-latching device.



(b) Phase-based D latch derives from bi-stable phase-based bit storage device (*e.g.*CMOS ring oscillator).



(c) Simulation results of phase-based D latch implemented as a CMOS ring oscillator.

Fig. 8. Design and implementation of phase-based D latch

Tying two such transparent D latches together results in an edge-triggered master-slave D flip-flop. With this we build a simplest FSM just to show a flavour of how computation systems operate in phase logic.

Fig. 9 shows a serial adder made of the D flip-flop and a full adder. Just as in the D latch, here we use only MAJORITY and NOT operations in the design for their simplicity of implementation using phase logic. We emphasize again that such a system can be realized using oscillators from various domains. Here we demonstrate its viability using CMOS ring oscillators only as an example and provide simulation results in Fig. 10. We add $a = 101$ with $b = 101$ sequentially during three clock cycles. From Fig. 10 we can see *cin* is held stable everytime CLK level is low (translates to having opposite phase as REF). During this time $cout = 101$ and $sum = 010$ can be read out sequentially. In the full system design their values can then be latched using other registers and connected to following stages in the system, or transformed to level-based logic if connected to other computation or display blocks.

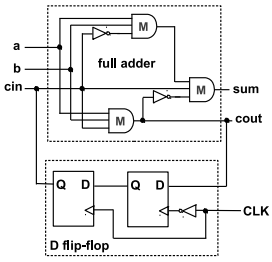


Fig. 9. Serial adder

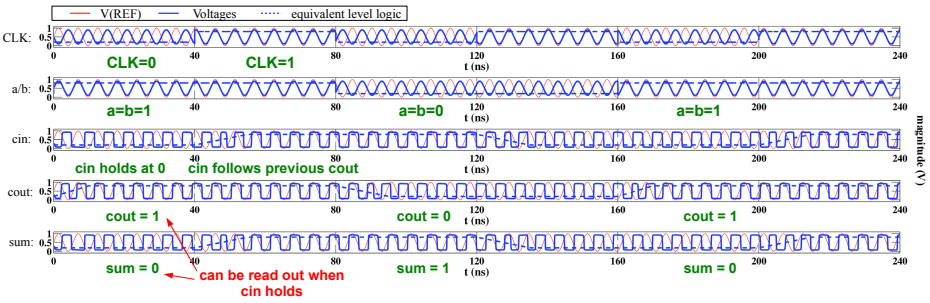


Fig. 10. Waveforms from adding $a = b = 101$ with serial adder in Fig. 9 implemented using ring oscillator

Even though our scheme is fundamentally different from the conventional computation framework in the way logic is encoded, as we have seen in the examples, the system-level design (FSM design) can be quite analogous to that of level-based logic systems. In this way, all the logic synthesis and timing analysis theories and tools can potentially still be used with only minor modifications, immediately enabling complex, large-scale system design based on phase logic.

3.4 Potential Power/Energy Advantages of PHLOGON

PHLOGON offers significant energy-efficiency benefits over von Neumann's original scheme. It uses continuously-running oscillators, which can be much more energy-efficient than von Neumann's latch-rings. Moreover, neither distribution

nor modulation of AC power is involved for running a PHLOGON architecture[11]. This reduces parasitic-related losses especially for large, intricately-routed systems, resulting in significant power savings over von Neumann's scheme.

Compared with level-based CMOS computation architecture, the circuits and nanodevice embodiments of PHLOGON can potentially still be considerably more energy efficient. Dynamic (capacitive charging/discharging) and continuous (sub-threshold leakage) power consumption in level-based CMOS are both strongly determined by the supply voltage. The lowest practical supply voltage today for level-based CMOS is about 0.8V; this number is unlikely to drop significantly in future years, due to threshold voltage, variability and noise barriers [37,38]. In contrast, ring oscillators in standard CMOS technologies operate in sub-threshold mode at supply voltages as low as 80mV [6,10,5]; while in III-V technologies, ring oscillators running at 0.23V were demonstrated almost 30 years ago [11]. 10× lower supply voltage translates to 100× lower dynamic (CV^2) power, and more than $20,000\times$ lower leakage power (exponential in supply voltage). We emphasize that these power savings result simply by moving from level-based to phase-based logic architectures, without any change in the underlying CMOS technology.

Such large power savings can result even with ring oscillators, which dissipate most or all of their energy every cycle. When harmonic oscillators, with Q factors appreciably greater than 1, are used, further energy savings[12] can be realized. On-chip CMOS LC oscillators with spiral inductors, though considerably larger in area than ring oscillators, are available today with Q factors greater than 10, making them an interesting candidate to explore for additional power efficiency. Integrated MEMS resonators, though even larger in area, feature Q factors of 10^4-10^5 [26], potentially making them extremely attractive for low power computation with easily available and well-developed conventional technologies. Resonant Body Transistor (RBT), a silicon-based resonator compatible with standard CMOS process, has been demonstrated to achieve >10GHz frequency with Q factor of 1830 [40], making it another promising candidate. Spin-torque nano-oscillators (STNOs) feature Q factors of more than 10^4 at frequencies of 25GHz [31,18,32]; as such, they offer very exciting power, as well as speed, possibilities.

4 Conclusions

In this paper we re-examined Goto and von Neumann's phase-based logic ideas and limitations of their previous implementations. We proposed enhancements to them, showing that almost any DC-powered, self-sustaining nonlinear oscillator can be used to build latches and combinatorial elements, enabling phase-based computing. We provided mathematical tools for analysing SHIL as the

[11] Note that SYNC and CLK can be weak, dissipating negligible power.

[12] *i.e.*, an energy advantage of roughly Q over ring oscillators using the same technology and supply voltage.

mechanism for phase-based logic encoding. We showed that phase logic offers inherent resistance to noise and variability and also discussed the potential energy-efficiency our scheme may achieve. These features have made PHLOGON an interesting and promising alternative to the conventional level-based computation architecture. We are currently exploring design details and tradeoffs involved in the practical manifestation of PHLOGON in post-CMOS and standard digital CMOS technologies.

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